

Portable Front-End Readout System for Radiation Detection

by

Maris Tali

THESIS
for the degree of
MASTER OF SCIENCE

(Master in Electronics)



Faculty of Mathematics and Natural Sciences
University of Oslo

June 2015

Det matematisk- naturvitenskapelige fakultet
Universitetet i Oslo

Acknowledgements

First of all, I would like to thank my advisor, Ketil Røed, for giving me the opportunity to write my master thesis on such an interesting and challenging subject as radiation instrumentation and measurement. I would also like to thank him for his insight and guidance during my master thesis and for the exciting opportunities during my studies to work in a real experimental environment.

I would also like to thank the Electronic Laboratory of the University of Oslo, specifically Halvor Strøm, David Bang and Stein Nielsen who all gave me valuable advice and assistance and without whom this master thesis could not have been finished.

Lastly, I would like to thank the co-designer of the system whom I worked together with during my master thesis, Eino J. Oltedal. It is customary to write that half of ones master thesis belongs to ones partner. However, this is actually the case in this instance so I guess 2/3 of my master thesis is yours and I definitely could not have done this without you. So, thank you very much!

Oslo, June 2015
Maris Tali

Contents

Acknowledgments	I
Glossary	VI
List of Figures	X
List of Tables	X
Abstract	XI
1 Introduction	1
1.1 Background and motivation	1
1.2 Goal of the thesis	3
1.3 Structure of the thesis	3
2 Theory	5
2.1 Ionizing Radiation	5
2.2 Radiation Sources	5
2.2.1 Common Modes of Radioactive Decay	6
2.3 Radiation Interactions With Matter	7
2.3.1 Stopping power	7
2.3.2 Range	10
2.3.3 Cross-Section Concept	10
2.3.4 Induced Fission	10
2.4 Radiation Effects in Electronics	10
2.4.1 Single Event Effects	10
2.4.2 Total Ionizing Dose Effects on MOS Transistors and Integrated Circuits	11
2.5 Detector Technology	13
2.5.1 Silicon Diode Detectors	13
2.5.2 Scintillation Detectors	15
2.5.3 Thin film breakdown counter	15
2.6 Detection of Ionizing Radiation	16

2.6.1	Alpha Particle Spectroscopy	16
2.6.2	Heavy Ion and Fission Fragment Spectroscopy	18
3	Design of the Front-End Electronics for Radiation Detection	19
3.1	General Readout Electronics for a Radiation Detector	19
3.2	Design Considerations for the Front-End Electronics	20
3.3	Analog card	21
3.4	Digital card	23
3.5	Design of the Preamplifier, Biasing Network and Test Input	25
3.5.1	Preamplifier	25
3.5.2	Choice of the Operational Amplifier for the Preamplifier	27
3.5.3	Bias Network	28
3.5.4	Test Input	29
3.6	Design of the Shaping Stage	29
3.6.1	Verification of the Design of the Preamplifier and Shaping Step	32
3.7	Design of the Differential Buffers	33
3.8	Choice of the ADC	34
3.8.1	Prototype ADC	34
3.8.2	Final design ADC	34
3.9	Design of Current Monitoring	36
3.10	Design of clock distribution	38
3.11	Design of the Power Network	39
3.11.1	Analog Card	39
3.11.2	Digital Card	39
3.12	Readout Electronics for a Thin Film Breakdown Counter	39
3.13	Window comparator	40
3.14	Choice between LVDS and CMOS as the signaling standard	41
3.14.1	Advantages and disadvantages of LVDS	41
3.14.2	Advantages and disadvantages of CMOS	41
3.14.3	Final choice of signaling	42
3.15	Layout of the PCB	42
3.15.1	Electromagnetic Compatibility considerations	42
3.15.2	Differential digital signaling layout considerations	43
3.15.3	Bypassing	43
3.15.4	Ground plane	43
4	Description of the Complete System and Software	45
4.1	Configuration of the FPGA	45
4.2	Embedded Linux on the FPGA	46
4.3	Software	47
4.3.1	Controlling the I2C Peripherals on the Digital Card	47

4.3.2	Clock	47
4.3.3	Current Monitors	48
4.3.4	Multiplexer	48
4.4	Main Program to Acquire Data from the System	48
5	Calibration and Testing of the System	51
5.1	Test equipment and Software Used	51
5.1.1	Function Generator	51
5.1.2	Power Supply	51
5.1.3	Oscilloscope	51
5.1.4	The PCB Design Software	52
5.1.5	Schematic Simulation	52
5.1.6	Data Analyzing and Plotting	52
5.2	Testing the analog card	52
5.2.1	Test setup for the analog card	52
5.2.2	Testing the preamplifier and shaping stage	52
5.3	Testing of the complete system	54
5.3.1	Test of Linearity of the System and Energy Calibration	54
5.3.2	Noise of the System	59
5.4	Radiation Spectroscopy with Radioactive Source	66
5.4.1	Test Setup	66
5.4.2	Pulse Pile-Up Considerations	68
6	Results	71
6.1	Notes on Channel 2	71
6.2	Alpha and Fission Fragment Spectroscopy with ^{252}Cf source	72
6.2.1	Energy Spectrum	72
6.2.2	Measured Intensity	72
6.3	Alpha Spectroscopy with ^{241}Am source	76
6.3.1	Energy Spectrum	76
6.3.2	Measured Intensity	79
6.4	Summary of Results of the Radiation Testing	79
6.5	Measured Energy Resolution of the System	79
7	Discussion and Conclusion	81
7.1	Discussion of the Design of a Portable System for Radiation Detection . . .	81
7.2	Discussion of the Characterization of the System with ^{241}Am and ^{252}Cf . .	82
7.3	Discussion of Using Different Types of Detectors and Detecting Various Types of Radiation	82
7.4	Suggestions for Future Improvements of the System	83
7.5	Conclusion	84

Appendices	A-I
Appendix A	A-II
Appendix B	B-I

Glossary

ADC Analog to digital converter. 34, 35, 38, 39, 43, 50

CMOS Complementary metal-oxide-semiconductor. III, 20, 34, 41, 42

FFT Fast Fourier Transform. VIII, 63–65

FPGA Field programmable gate array. XI, 20, 23, 24, 34, 35, 37–40, 42, 50, 51, 54, 58, 61, 63

FWHM Full Width at Half Maximum, Corresponds to 2.35σ in a normal distribution. 63, 82

GPIO General Purpose Input/Output. 42

HSMC High Speed Mezzanine Connector. 42

IC Integrated circuit. 11, 24, 36

LED Light Emitting Diode. 38

LET Linear Energy Transfer. 9

LVDS Low-voltage differential signaling. III, 34, 41, 42

NIM Nuclear Instrumentation Module. 1

PIN p - i(intrinsic) - n. 14

TID Total Ionizing Dose. 12

List of Figures

1.1	A typical NIM crate setup for coincident radiation counting [Private photo from the author]	2
2.1	Total Stopping power for protons(p+), electrons (e^-) and α particles in air(dry, sea level) from ESTAR, PSTAR and ASTAR databases [1]	9
2.2	A thin-film breakdown counter. a) contact area, b)detector area c) connectors	16
2.3	Americium 241 energy spectrum from [2]	17
2.4	Californium 252 main alpha energy spectrum from [3]	18
3.1	Schematic of general electronics for detection of radiation using a silicon detector	19
3.2	Block diagram of the general components of the analog and the digital card	21
3.3	Assembled analog card with different connectors marked. Green: RJ45 connector for the differential signal to the digital card, Blue: Power connector for the ± 5 V, White: Bias voltage for the detectors (90 V), Red: Current monitoring connections, Yellow: Inputs for detectors	22
3.4	Slow channel of the analog card	22
3.5	Assembled digital card with different connectors marked. Yellow: RJ45 connector for the differential signal from the analog card, Blue: Single-ended input to the on-board differential buffer, White: Digital inputs to the window comparators, Red: Current monitoring connections, Green: Connector to the FPGA (connector on the bottom side of the card)	23
3.6	The digital card. The number on the connections shows the number of signals.	25
3.7	Preamplifier configurations: (a) Current-sensitive preamplifier, (b) Voltage-sensitive preamplifier, (c) Charge-sensitive preamplifier	26
3.8	Preamplifier ADA4817 with detector bias network, with two tested feedback configurations and typical signal before and after amplification	27
3.9	Shaping stage with a simple differentiating step and a Sallen-Key integrating step, with typical signal in to and out of the shaping stage	30
3.10	LTSpice simulation of a signal after the differentiating step, using the schematic in figure 3.11 with and without pole/zero cancellation resistor	31

3.11	Schematic of the test circuit with a preamplifier and shaping stage used in LTSpice. Signal from different stages shown for two 1 MeV equivalent pulses.	33
3.12	Connections of the differential buffer LTC6409 with gain 1 V/V	34
3.13	The inputs of the ADC LTC2283	35
3.14	Connections of Channel 2 of INA3221 with a shunt resistor R_S . Source: [4]	37
3.15	Schematic of the connections of the adjustable regulator LM317 to generate 1.5 V	39
3.16	Typical readout electronics for a TFBC interfaced with an FPGA	40
3.17	Window comparator, with high trigger voltage V_{HIGH} and low trigger voltage V_{LOW}	41
3.18	All of the PCBs designed and assembled for this thesis. From top to bottom: 1) First prototype, analog and digital parts on the same card 2) Analog test, test for 3 different preamplifiers, 3) Final analog design 4) Final digital design	44
4.1	Block schematic of the complete system for radiation detection	45
4.2	The Java program used to control and acquire data from the system described in this thesis	49
5.1	Response of the preamplifier and shaping stage to a 1 MeV charge equivalent. a) signal after preamplifier, b) after the differentiating stage, c) after integrating stage	53
5.2	Response of the fast channel, channel 2, preamplifier and differential buffer with gain $G = 2$ to a 1 MeV charge equivalent. a) signal from preamplifier b) signal from differential buffer (AC connected to probe, + output)	54
5.3	Test of linearity for channel 1 and channel 2, with trigger level 20 and channel 1 with trigger level 40	57
5.4	The shift in pulse heights when different baseline trigger levels are used . .	59
5.5	Example of inherent noise on top of a signal with equivalent charge of 10 MeV sampled with 2.5 GSps with an oscilloscope and with 125 MSps with the system described in this thesis.	60
5.6	The power spectral density from data acquired from the analog card with the averaged difference between the two signals, plotted up to 20 MHz to demonstrate the effect of connecting the detector on lower frequency noise .	62
5.7	Histogram of 100000 stable test pulses sent into the slow channel, channel 1, with $C_F = 1$ pF with equivalent charge of 1 MeV. Line plot of oscilloscope probe connected to the output of channel 1. Also marked constants for energy resolution calculations used in section 6.5	64
5.8	FFT of the noise signal on Channel 1 of the analog card with the the FPGA powered on and powered off. Plot on right zoomed in on 125 MHz	65
5.9	Schematic of the setup of the system described in this work for radiation testing	68

5.10	Schematic of setup of the Californium source. Not to scale	68
5.11	Schematic of setup of the Americium source. Not to scale	68
5.12	Tail pile-up effects. Top: pile-up on the tail of the preceding pulse, bottom: pile-up on the undershoot of the preceding pulse from [2]	69
5.13	Raw pulse from ^{252}Cf source acquired with channel 1 of the system described in this work, example of peak pile-up	70
5.14	Spectral effects of peak and tail pile-up from [2]	70
6.1	^{252}Cf source. Pulses read out channel 2. Signal is marked with an arrow. The high frequency noise is visible, signal processing on the FPGA is turned off	72
6.2	^{252}Cf source. A pulse read out channel 1 from the FPGA with height of 324 ADC data points which corresponds to charge 6.1 MeV. Baseline trigger is set to 40	73
6.3	^{252}Cf source. Pulses read out channel 1, a tail pile-up is also visible and is marked with an arrow. Zero suppression and baseline correction are applied. Baseline trigger is set to 40	73
6.4	Californium 252 energy spectrum, logarithmic Y axis, acquired with channel 1, 5E4 pulse heights. Baseline trigger is set to 40	74
6.5	Californium 252 energy spectrum, logarithmic Y axis, acquired with channel 1, 5E4 pulse heights, zoomed in on main lobe, plotted with normal fit. Baseline trigger is set to 40	74
6.6	Californium 252 energy spectrum, linear Y axis, acquired with channel 1, 5E4 pulse heights, zoomed in on main lobe, plotted with normal fit. Baseline trigger is set to 40	75
6.7	Plot of data acquired from channel 1 from ^{252}Cf source, 1E6 points, all digital signal processing turned off, events marked with arrows. Baseline trigger is set to 40	76
6.8	^{241}Am source. Pulses read out channel 1. Zero suppression and baseline correction are applied. Baseline trigger is set to 40	77
6.9	Complete Americium 241 energy spectrum, logarithmic Y axis, acquired with channel 1, 2E5 pulse heights, 5000 counts at the main lobe center . . .	77
6.10	Americium 241 energy spectrum, logarithmic Y axis, acquired with channel 1, 2E5 pulse heights, 5000 counts at the main lobe center, zoomed in on the main lobe	78
6.11	Americium 241 energy spectrum, linear Y axis, acquired with channel 1, 2E5 pulse heights, 5000 counts at the main lobe center, zoomed in on the main lobe	78
6.12	Plot of data acquired from channel 1 from ^{241}Am source, 1E5 points, all digital signal processing turned off, events marked with arrows. Baseline trigger is set to 40	79

A.1	Connector for current measuring on the digital card.	A-II
A.2	Connector for the FPGA on the digital card.	A-III

List of Tables

2.1	Summary of variables used in equation 2.2	8
3.1	ADC settings	36
4.1	Devices on the digital card connected to the I2C-0 on the embedded Linux	47
5.1	Measurements obtained during the calibrations of the channels, baseline trigger level 20	55
5.2	Theoretical properties of the system calculated from the calibration equations	56
5.3	Measurements obtained during the pulse height shifting calibration, values in ADC data points	58
5.4	Properties of the two radiation sources used for system characterization . .	67

Abstract

In this master thesis the front-end electronics for a complete portable system for radiation detection has been studied and designed, the other half of the system has been described in [5]. Traditionally, the electronics used in radiation detection are expensive, complicated to set up and use and not portable. The aim of this master thesis was therefore to build an easy to use and set up and portable radiation detection system. The result is two electronics cards interfaced with an FPGA (field programmable gate array) running an embedded Linux system. The system uses a socket server to talk to a user interface program written in Java.

The resulting system has been verified by both simulation and testing with a pulse generator and radiation sources.

Chapter 1

Introduction

1.1 Background and motivation

The foundation of all radiation measurements is the combination of one or more radiation sources and one or more radiation detection units. [6] Traditionally radiation measurement equipment is highly specialized, expensive and not portable. Many of the systems are permanently installed at radiation detection facilities and are locked down to a specific type of detector or radiation. An example of a commonly used system for radiation detection is the so called NIM crates or nuclear instrumentation module crates. [6] These are large rack mounted systems where each module has a specific, narrow purpose. Although these crates are very widely used for counting and pulse height analysis, they are time consuming to first set up, very expensive and not versatile outside of the one or more function that a specific module has.

A typical NIM crate can be seen in figure 1.1 with two quad counter-timer modules, a level adapter, a coincidence module and 3 dual timer modules. The crate in the picture does not include a pulse height analyzer, which is a separate module. In addition to this, a separate preamplifier is needed to interface detectors with this system.

The aim of this master thesis is to develop electronics optimized to read out and analyze the charge which is generated in a silicon particle detector by nuclear reaction products or an alpha-particle emitting radioactive source during laboratory testing. As testing of silicon detectors often is done at various facilities and existing systems are large, expensive and not easily portable, it is desirable to make this readout electronics as compact, easy to use and portable as possible. The custom design enables both tailoring the system to specific types of radiation and generalization for different detector types and different measurement, such as current monitoring. It will also be of interest to develop this readout electronics for the purpose of laboratory use at UiO.

The system can also be used as a general setup where silicon detectors can be tested and characterized using for example an alpha particle emitting radioactive source. Such a

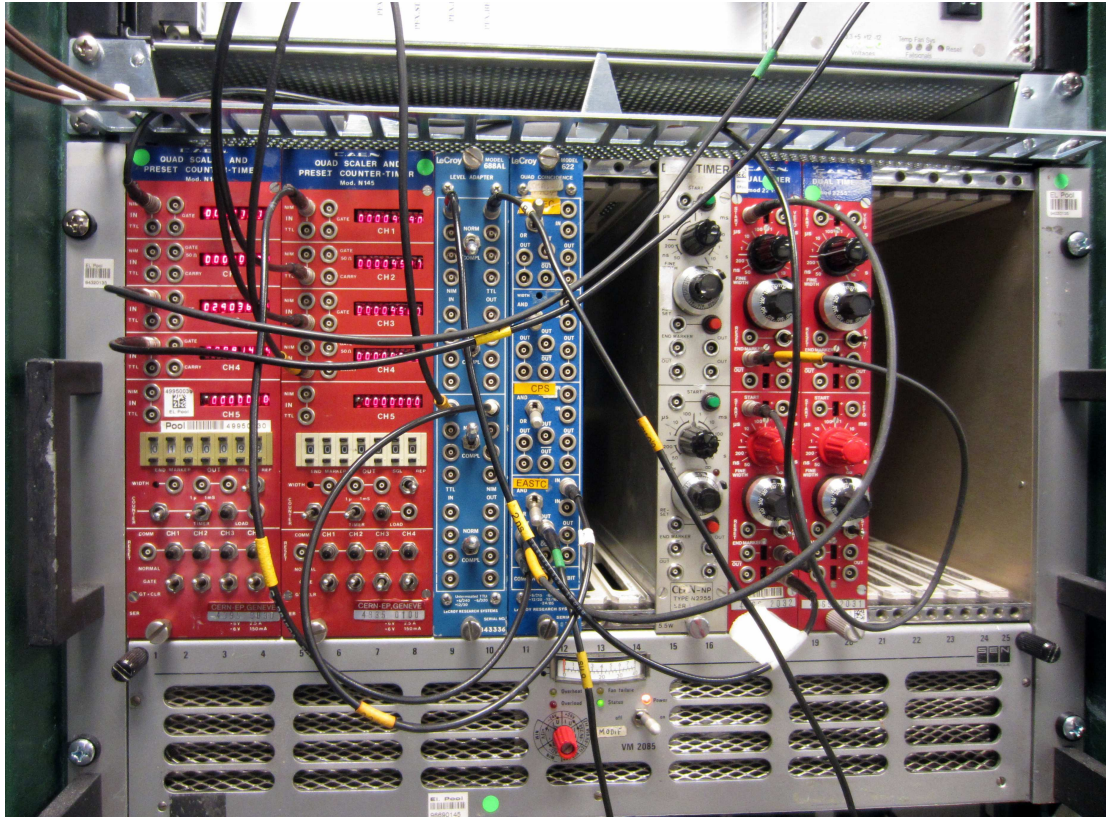


Figure 1.1: A typical NIM crate setup for coincident radiation counting [Private photo from the author]

setup could even provide a highly relevant laboratory exercise for students learning about radiation detection and related readout electronics.

The development from this project will also be relevant for other applications. This thesis discusses the possibility of using the system used in conjunction with a thin-film breakdown counter and a uranium target as a beam flux monitor at cyclotrons.

1.2 Goal of the thesis

The main goal of the thesis is the characterization and design of a compact electronic data acquisition system for detection of radiation. This major goal can be divided into minor goals, which can be summarized as follows:

- Design analog front-end electronics to interface a silicon PIN detector to the digital signal processing back-end
- Develop the system to the level of being plug-and-play, with both electronics and software being easy to set up and use
- Characterize the system using alpha sources Americium 241 (^{241}Am) and Californium 252 (^{252}Cf)
- Discuss the possibility of using different types of detectors and detecting various types of radiation with the system described in this thesis

1.3 Structure of the thesis

Chapter 1 Introduction

Introduction to the thesis and motivation for the work done in the thesis.

Chapter 2 Theory

Theory of radiation and its interaction with matter. Explanation of how these interactions enable detection with different types of detectors. Introduction to most common types of detectors and types of radiation most commonly used to measure with them. A summary of both cumulative damage and single event radiation effects in electronics.

Chapter 3 Design of the Front-End Electronics for Radiation Detection

A summary of different electronic building blocks that commonly make up a radiation detection and measurement systems. Detailed description of the electronic system designed in this work.

Chapter 4 Description of the Complete System and Software

Description of the electronic front-end described in this work together with the FPGA readout system described in a thesis by E. J. Oltedal [5]. Short overview of software written to communicate with the electronic system run both on the FPGA and on a separate PC for data acquisition.

Chapter 5 Calibration and Testing of the System

Description of the instruments and software used for the testing and characterization of the system. Summary of sources of noise in the system and tests for both the analog card and complete system. Description of the test setup for measurements with real radiation sources.

Chapter 6 Results

Description of test setup for and results of characterization of the system with alpha sources Americium 241 (^{241}Am) and Californium 252 (^{252}Cf)

Chapter 7 Discussion

Discussion of results obtained in chapter 6 and evaluation if the work done in this thesis was sufficient to reach the goals set. Discussion of possible future improvements of the system.

Appendix A

Appendix A contains schematics for the electronics of the system.

Appendix B

Appendix B contains program code written to control the some of the integrated circuits in the system:

- mux.c - to control the multiplexer on the digital card
- clock.c - two of the most important functions in the program to control the clock circuit on the digital card

Chapter 2

Theory

2.1 Ionizing Radiation

Radiation with sufficient energy to ionize atoms in matter is called ionizing radiation. Radiation emitted when an unstable nucleus in an element, a radioisotope, disintegrates, is called nuclear radiation. [6]

Radioactive decay, also referred to as disintegration, is a spontaneous change within the nucleus of an atom, that results in the emission of particles and electromagnetic radiation. The mass of the product, the daughter, is always less than that of the original nuclide, the parent. Simply put, a nuclide's radioactivity is determined by the ratio of Z (the atomic number of an atom) to N (number of neutrons in an atom). For low- Z elements the stable nuclides are found at $Z=N$, whereas for higher Z values N becomes greater than Z . [6].

The activity of a radioisotope source is defined as its rate of decay. The historical unit of activity has been curie (Ci), defined as 3.7×10^{11} disintegrations per second. More commonly used is its SI equivalent, the becquerel (Bq), defined as $2.703 \times 10^{-11} Ci$. A given radiation will be emitted only as a fraction of all decays, so knowledge of the decay scheme of the particular isotope is necessary to infer a radiation emission rate from its activity. The decay of a given radioisotope may lead to a daughter product whose activity also contributes to the radiation yield from the source. [2]

The unit for radiation energy is the electron volt (eV), defined as the kinetic energy gained by an electron by its acceleration through a potential difference of 1 volt. [2]

2.2 Radiation Sources

Radiation sources that are relevant for radiation detection can be divided into the following general types:

- Charged particulate radiation:

- Fast electrons
- Heavy charged particles
- Uncharged radiation
 - Electromagnetic radiation
 - Neutrons

Fast electrons include beta particles emitted in nuclear decay, as well as energetic electrons. Heavy charged particles include all energetic ions with a mass of one atomic mass or greater, such as alpha particles, protons and fission products. Electromagnetic radiation includes X-rays and gamma rays. Neutrons generated in various nuclear processes are the last major category. [2].

2.2.1 Common Modes of Radioactive Decay

Some common modes of decay are the following :

- Beta Decay
 - Negative Beta Decay (Negatron Emission)
 - Positive Beta Decay (Positron Emission)
 - Electron Capture
 - γ Radiation Following β Decay
- Alpha Decay
- Spontaneous Fission

Only modes of decay that are relevant for this thesis are discussed.

Alpha Decay

The most common decay mode in high-Z nuclides is Alpha decay. The alpha decay can be schematically described as:

$${}^A_Z X = {}^{A-4}_{Z-2} Y + {}^4_2 \alpha \quad (2.1)$$

where X and Y are the initial and final nuclear species. The alpha particles appear, for all practical purposes, mono-energetic. For each distinct transition between initial and final nucleus, a fixed energy difference or Q-value characterizes the decay. Most alpha particle energies are limited to between 4 and 6 MeV. The most common α source is ^{241}Am , which is also well suited for calibrating solid-state detectors. [2] This source was used to characterize the readout electronics in this work. The testing is discussed in more detail in section 6.3.

Spontaneous Fission

Fission is a process in which a heavy nucleus breaks down into lighter nuclei. [2] Fission can either be induced or spontaneous. Induced fission is discussed in detail in section 2.3.4.

Spontaneous fission is a rare process except for extremely heavy nuclei. This is because of the energy barrier that needs to be overcome. The most widely used source that undergoes spontaneous fission is ^{252}Cf . However, the probability of alpha decay is much greater than that of spontaneous fission. Spontaneous fission process is the only spontaneous source of energetic heavy charged particles with mass greater than that of the alpha decay. Fission fragments are therefore used in the calibration and testing of detectors intended for general application to heavy ion measurements. [2] This source was also used to characterize the readout electronics in this work. The testing is discussed in more detail in section 6.3.

2.3 Radiation Interactions With Matter

The types of radiation mentioned in section 2.2 are divided into charged radiations and uncharged radiations. The charged radiations continuously interact through the coulomb force with the electrons present in any medium through which they pass. The uncharged radiation is not subject to the coulomb force. Instead, these radiations interact only with the nucleus of the material they pass through. If the interactions do not occur within the detector, these uncharged radiations can pass completely through the detector volume undetected. [2]

2.3.1 Stopping power

Heavy Charged Particles Interactions

The linear stopping power S for charged particles, also known as specific energy loss or rate of energy loss, in a given absorber is defined as the differential energy loss for that particle within the material divided by the corresponding differential path length $S = -dE/dx$. [2] Unless the particle is highly relativistic, ionization is the main electromagnetic contribution to the energy loss for moderately relativistic charged particles other than electrons. If the incident particle velocity β_c is larger than that of orbital electrons and small enough that radiative effects do not dominate (for example pion energy smaller than 100–200 GeV), then the mean energy loss (or stopping power) is given by the Bethe-Bloch equation [7]

$$-\frac{dE}{dx} = Kz^2 \frac{Z}{A} \frac{1}{\beta^2} \left(\frac{1}{2} \ln \frac{2m_e c^2 \beta^2 \gamma^2 T_{max}}{I^2} - \beta^2 - \frac{\delta}{2} \right) \quad (2.2)$$

where T_{max} is the maximum kinetic energy which can be imparted to a free electron in a single collision, the other variables are defined in Table 2.1. For a given non-relativistic

Symbol	Definition	Units or Value
dE	Differential energy loss	
dx	Differential path length	
β	Projectile velocity	units of c_0
γ	$1/\sqrt{1 - \beta^2}$	
c_0	Speed of light in vacuum	$299\,792\,458\,\text{m s}^{-1}$
z	projectile charge	e
K	$4\pi r_e^2 m_e c^2 N_A$	$0.307\,\text{MeV cm}^2/\text{mol}$
m_e	Electron rest mass	$0.511\,\text{MeV } c_0^{-1}$
N_A	Avogadro's number	$6.022 \times 10^{23}\,\text{mol}^{-1}$
A	Atomic mass of the medium	g mol^{-1}
Z	Atomic number of the medium	
I	Mean excitation energy	eV
δ	Density effect correction to ionization energy loss	

Table 2.1: Summary of variables used in equation 2.2

particle the dE/dx varies as β or particle energy. Particles of the same velocity have very similar rates of energy loss in different materials; there is a slow decrease in energy loss with decreasing Z . [7]

Fast Electrons Interactions

When compared with heavy charged particles, fast electrons lose their energy at a lower rate in the absorber material. The specific energy loss due to ionization and excitation for fast electrons is denoted $(-dE/dx)_c$. Fast electrons also lose energy through radiative processes called bremsstrahlung or electromagnetic radiation. Deflections of the electron in its interaction with the absorber radiates energy $(-dE/dx)_r$. Radioactive losses are most important for high electron energies and materials of high atomic number. The total linear stopping power for electrons is the sum of the collisional and radioactive losses $dE/dx = (dE/dx)_c + (dE/dx)_r$. [2] Total stopping power comparison in air between protons,

electrons and alpha particles in air can be seen in figure 2.1.

Fission Fragments Interactions

The heavy fragments produced as a result of spontaneous or induced fission of heavy nuclei differ from previously mentioned charged particles. They have a very large effective charge which results in a greater specific energy loss. Because the initial energy is so high, the range of a typical fission fragment is smaller than that of an α particle. [2]

Fission fragment specific energy loss decreases as the particle loses energy in the absorber. This behavior is the result of continuous decrease in the effective charge carried by the fragment as its velocity is reduced. The pickup of electrons begins immediately at the start of the track and therefore the factor z , projectile charge, in the numerator from equation 2.2 continuously decreases. The decrease of the specific energy loss is large enough to overcome the increase that usually accompanies a reduction in velocity. [2]

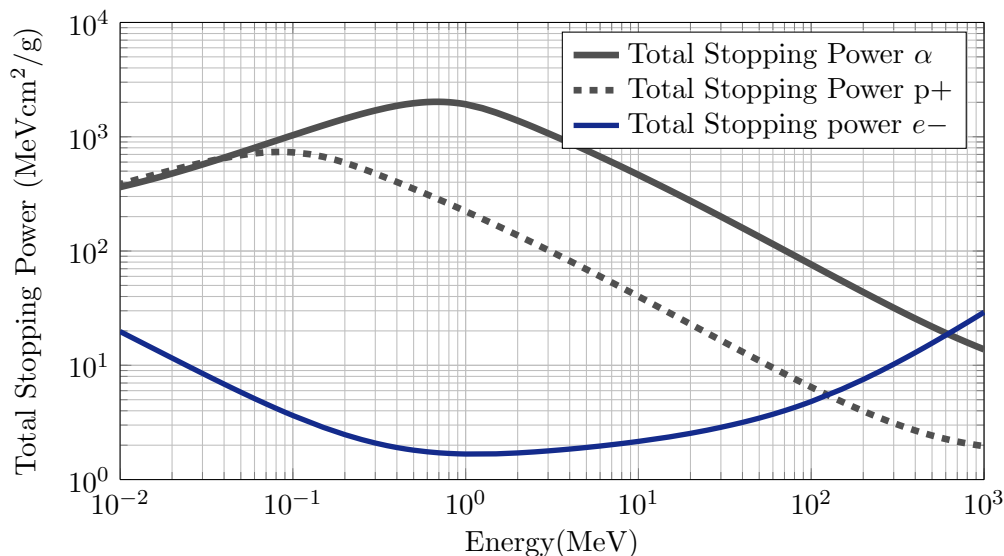


Figure 2.1: Total Stopping power for protons(p+), electrons (e^-) and α particles in air(dry, sea level) from ESTAR, PSTAR and ASTAR databases [1]

Restricted Linear Energy Transfer (LET)

Linear energy transfer is closely related to specific energy loss. Practical detectors often measure the energy deposited, not the energy lost. When energy is carried off by energetic electrons, it is more appropriate to consider the mean energy loss excluding energy transfer

greater than some cutoff energy T_{cut} . If T_{cut} is infinite, linear energy transfer is identical to stopping power. [7]

2.3.2 Range

An important property of particles is their Range R in absorbers. This may be defined as the total path length a particle travels in an absorber until it loses all its energy. By integrating the specific energy loss with respect to energy we get the continuously slowing-down approximation or CSDA. [6] The average depth to which a particle will penetrate measured along the initial direction of the particle is projected range. [2]

2.3.3 Cross-Section Concept

The probability of a particulate event occurring between a neutron and a nucleus is expressed through the concept of the cross section. If a large number of neutrons of the same energy are directed into a thin layer of material, some may pass through with no interaction, others may have interactions that change their direction and energies, and some may not pass the sample at all. There is a probability for each of these events. For example, the probability of a neutron being absorbed is the probability of neutrons being absorbed divided by the number of target atoms per unit area of the layer. The cross section has the dimension of the area. Because this type of cross section describes the probability of neutron interaction with a single nucleus, it is called the microscopic cross section. [8]

2.3.4 Induced Fission

An interaction that is appropriate to mention is induced fission. Fission is relevant for this work due to its ability to induce SEUs and as a mechanic used to measure radiation in the thin film breakdown counter discussed in section 2.5.3. In the case of induced fission, the parent nucleus is bombarded with a neutron. If the parent absorbs the neutron, the neutron binds to the parent, releasing energy. This energy could be more than the potential energy barrier for fission. If this is not the case, the incident neutron needs to have a minimum kinetic energy in order to be able to induce fission. [9] Nuclear fission emits both neutrons, photons, protons and light nuclei such as alpha particles. Energy released in nuclear fission is also sufficient for pion production. [10]

2.4 Radiation Effects in Electronics

2.4.1 Single Event Effects

As the density and functionality increases and power decreases, electronics sensitivity to radiation increases dramatically. There are different types of radiation damage in semicon-

ductor devices varying from data disruptions to permanent damage. Single event effects (SEE) are device failures induced by a single radiation event. [11]

Single Event Upset

Single event upset (SEU) occurs when a radiation event causes enough of a charge disturbance to reverse or flip the data state of a memory cell. The device is not permanently damaged by the radiation, if new data is written to the bit it will be stored correctly. The error can occur in a critical system control register such as that found in FPGAs or dynamic random access memory (DRAM) control circuitry, so that the error causes the product to malfunction. [11] Since the FPGA configuration is stored in the SRAM of an FPGA, an SEU might change the stored configuration and cause unexpected behavior.

This type of effect is relevant to the data acquisition system discussed in this thesis because of the use of the Cyclone V based FPGA, which has logic blocks in SRAM memory, as the digital data processing back-end [12].

Single Event Latchup

Single event latchup (SEL) is an unintentional short circuit between components on an integrated circuit causing malfunction. A latchup causes a bit-flip to be permanent. The circuit has to be powered down to correct this effect. [13]

Single Event Burnout

In the case of a single event burnout, the current in a SEL is not limited and device may be destroyed. This is the most harmful form of single event effect to electronics, since the failure is permanent. [13]

Single Event Transients

Single event transient (SET) is a current or voltage spike, which may propagate through logic gates and produce system failures. If this spike is captured by a storage element, the SET becomes an single event upset. [13]

2.4.2 Total Ionizing Dose Effects on MOS Transistors and Integrated Circuits

Radiation-induced oxide and interface trapped charges affect the performance and reliability of MOS transistors and integrated circuits (ICs) to varying degrees depending on a number of operational conditions. [14]

Threshold Voltage Shift in Transistors

Threshold voltages for both N- and P-channel MOS transistors shift due to radiation-induced trapped oxide charge and trapped interface charge. The contributions are additive for P-channels and subtractive for N-channel MOS transistors. Total ionizing dose (TID) induced threshold voltage shifts depend on oxide thickness. [14]

Transconductance or Gain of the Transistors

The transconductance of the MOS transistor is decreased by radiation-induced reduction in carrier mobility in the device channel caused by charges trapped at the silicon/silicon dioxide interface. Transconductance can also be decreased by increases in surface resistivity. [14]

Channel and Junction Leakage Current and Breakdown

Gate-induced drain leakage current is increased by TID. Trapped charge buildup in lateral oxide isolation regions increases transistor edge leakage current and changes junction breakdown voltage. [14]

Noise in Transistors

Especially 1/f noise is increased by TID. The radiation-induced noise has been correlated with oxide-trapped charges and interface trapped charges. [14]

Effects in Integrated Circuits

TID radiation effects impact both DC and AC-parameters and functionality of integrated circuits. The DC-parameters include quiescent supply current (standby-current), noise margin and output drive levels. The AC-parameters include rise- and fall time and propagation time. These factors are affected by dose, dose rate, device design and operating temperature. The principal-causes of radiation-induced circuit failure is an inability to switch from one state to another and increases in standby power. The four following radiation-induced failure modes are responsible for IC performance degradation:

- Power related failure due to leakage current increasing standby power over a limit
- Increased N-channel leakage current combined with decreased P-channel drive generates nodes in indeterminate logic states
- Delays along a signal path are too large for synchronous operation
- Increases in P-channel threshold voltage inhibit switching

Functional failure in CMOS ICs due to TID exposure at dose rates greater than 5Sv/s or 500 rad/s is usually preceded by a rapid increase in standby current, due to oxide trapped holes. [14] Due to this fact, failure of the ICs can be predicted by the change in current draw of the IC. Current monitoring is therefore a useful tool in estimating IC performance in high-dose environments. Design of such a circuit is discussed in chapter 3.9.

2.5 Detector Technology

2.5.1 Silicon Diode Detectors

Silicon diodes have become the most popular type of detectors for detection of heavy charged particles. They are often used for alpha particle and fission fragment spectroscopy. The advantages of silicon detectors are [2] :

- good energy resolution
- good stability
- excellent timing characteristics
- very thin entrance window
- simplicity of operation

Ionizing Radiation Reaction with Semiconductors

When a charged particle passes through a semiconductor many electron-hole pairs are produced along the track of particle. If an electric field is applied to the semiconductor, both the electrons and holes will undergo a net migration. The motion will be a combination of random thermal velocity and net drift velocity parallel to the direction of the applied field. Electrons move in the opposite direction of the applied electric field while holes move in the direction of the applied electric field. In silicon and germanium mobility of holes and electrons are roughly of the same order. At lower electric field values the drift velocity is proportional to the electric field. At higher electric field values, the drift velocity increases slower with the increase of the field until it reaches a saturation velocity. Here the velocity becomes independent of the electric field increase. [2]

Pulse Rise Time

Many detectors are operated with electric fields high enough to result in saturated drift velocities to make the collection of charge carriers fast. This way, rise time of the signal pulse will roughly be under 10 ns for typical detectors. The total detector contribution to the rise time is composed of charge transit time and plasma time. [2]

Charge transit time is the time for migration of electrons and holes formed by the incident radiation across the region of high electric field in the depletion region. In totally depleted detectors. The depletion width is fixed by the physical thickness of the silicon wafer and therefore the transit time is decreased when the bias voltage is increased. [2]

Plasma time is observed when the radiation is heavy charged particles. The density of the electron hole pairs is then enough to form a plasma-like cloud of charge that shields the interior from the electric charge. The plasma time is defined as the time required for the cloud to disperse and normal charge collection to begin. [2]

The dominant advantage of semiconductor detectors over gas-filled detectors is the amount of ionization energy required to create an electron-hole pair, which is 3.6 eV for silicon compared to about 30 eV for gas. Because of this, the statistical fluctuation in the number of carriers per pulse becomes a smaller fraction of the total and the greater amount of charge per pulse leads to a better signal to noise ratio. [2]

P-N Junction and Reverse Biasing

The junction of p-doped and n-doped silicon, generally known as a diode configuration, has many favorable properties. The concentration of electrons is much higher in n-type region. The discontinuity in electron density causes a net diffusion of from regions of high concentration to lower concentration regions. This causes a net negative space charge in the p-region and a net positive space charge on the n-region. This region is called the depletion region and it extends to both n- and p-region.

When a reverse bias is applied to the region, virtually all the applied voltage will appear across the depletion region, since its resistivity is much higher than that of a normal n- and p-type material. Reverse biasing also increases the size of the depletion region because of the accentuated difference across the junction. The diode detectors are therefore biased with the largest possible voltage so that the detector is fully depleted but under the breakdown voltage, which could destroy the semiconductor detector. [2]

Silicon PIN Detector

The type of detector used in this work is called a silicon PIN detector. In this detector configuration a high-resistivity i-region is provided with p and n noninjecting contacts at either surface to help reduce the leakage current to below that which would be observed with a simple diode. A typical thickness of 300 μm is sufficient to provide useful detection efficiency up to 20 or 30 keV. [2]

Detector Noise and Resolution

The main contributions to the semiconductor detector noise are fluctuations in bulk generated leakage current, fluctuations in the surface leakage current and noise with series

resistance and poor electrical contacts. The importance of these sources will depend on the detector leakage currents, detector capacitance and depletion level of the detector.

Even in the absence of ionizing radiation, all detectors will show some finite conductivity and therefore a steady-state leakage current will be observed. Random fluctuations in the leakage current represent a significant source of noise in many situations. The rate of thermal generation of electron-hole pairs is increased by the increase of the depletion region and reduced by the cooling of the detector. [2]

2.5.2 Scintillation Detectors

Scintillation is the process of producing light. Scintillation radiation detectors convert light to an electrical pulse. Although scintillation is one of the oldest techniques for radiation detection, many modern detectors exist that use this principle. There are different types of scintillating materials, the most important being:

- Organic Scintillators
- Inorganic Scintillators
- Unactivated and Activated Fast Inorganics
- Transparent Ceramic Scintillators
- Glass Scintillators
- Noble Gas Scintillators

The scintillation process works by converting a small fraction of the kinetic energy lost by a particle in a scintillator into fluorescent energy. The fraction of the energy converted depends on both the type of particle and its energy. Because of the dependence of the type of particle, the absolute light yield of a scintillator is described by MeV electron equivalent (MeVee). The energy required to generate 1 MeVee is 1 MeV for fast electrons but can be several electron volts for heavy charged particles. [2]

2.5.3 Thin film breakdown counter

Thin film breakdown counters offer immediate information on particle fluxes, require relatively low voltages (compared to for example scintillating detectors) and are simple, compact and inexpensive. [15]

The thin film breakdown counter is a thin-film capacitor in which heavy fission fragments induce non-shortening breakdowns. The thin-film capacitor can be a metal-insulator-silicon sandwich or a metal-insulator-metal structure deposited on a glassy or ceramic substrate. An example of such a detector can be seen in figure in figure 2.2. It consists of

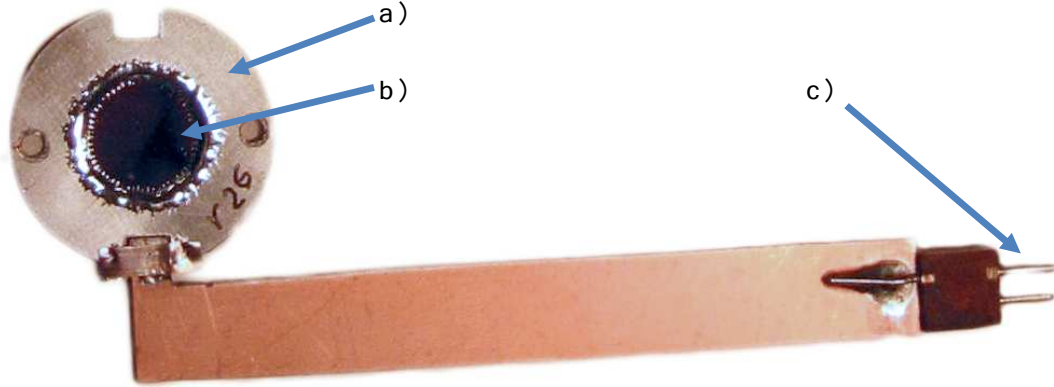


Figure 2.2: A thin-film breakdown counter. a) contact area, b) detector area c) connectors

the detector area where the breakdown occurs and the contact area which has a reinforced insulation. [15]

At least one of the electrodes is thinner than 1000 \AA . With such electrodes the breakdowns are non-shorting because the destructive process is mainly vaporizing and not melting. It is customary to insert a resistor larger than $10 \text{ k}\Omega$ between the power source and the capacitor to prevent larger destruction by propagation of breakdowns. The breakdowns are then single-hole types. The breakdown vaporizes a hole in the oxide and a much larger hole in the top electrode and therefore the top electrode remains isolated from the silicon [15]. The typical readout and biasing electronics are described in chapter 3.12. To use in detection, the detector is biased to a certain predetermined voltage level where breakdowns occur and whenever a breakdown-induced voltage spike is generated, it is compared to a threshold and then counted. To use the thin film breakdown counter to measure beam flux, a uranium target is used in front of the detector, and the resulting fission fragments are counted. This is an induced fission process described in 2.3.4.

2.6 Detection of Ionizing Radiation

2.6.1 Alpha Particle Spectroscopy

silicone diodes operated at room temperatures are near-ideal detectors for alpha particles and other light ions. The performance of semiconductor detectors conventionally is tested by recording the pulse height spectra of a monoenergetic alpha source. The most common of these is ^{241}Am , the corresponding spectrum can be used to compare solid-state detectors. [2] This source was also used in this work. A spectrum of ^{241}Am taken with a good resolution detector can be seen in figure 2.3.

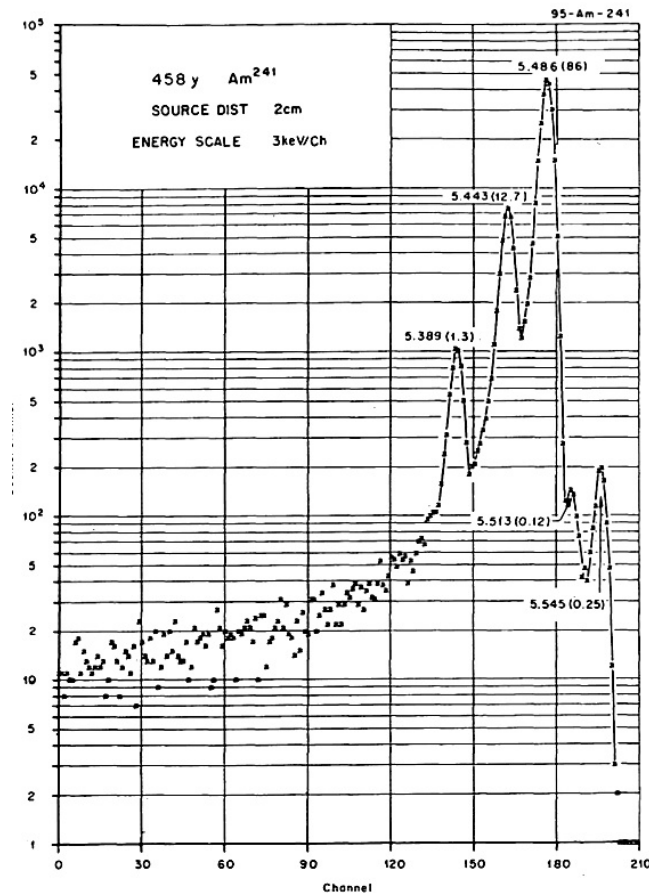


Figure 2.3: Americium 241 energy spectrum from [2]

With alpha particles in the 5 MeV energy range, the noise contribution of the preamplifier and the other electronic components can be much smaller than the inherent energy resolution of the detector itself. The statistics of the carrier charge formation limits the energy resolution achievable. For silicon the predicted statistical limit is $FWHM_{lim} = 3.47$ keV at the Americium 241 main alpha component with $E = 5.486$ MeV. In commercially available detectors, the energy resolution tends to be not better than 10 keV. One of the reasons for the difference in the predicted and the actual limit is that a small portion of the alpha energy is transferred to recoil nuclei rather than the electrons. It has been estimated that this effect accounts for about 3.4 keV for 6 MeV alpha particles. Other significant contributions to peak broadening are the effects of incomplete charge collection and variations of the energy lost by the particle in dead layers at the detector surface. For lower particle

energies and detectors with higher capacitances, electronic noise can also be a significant contribution to peak broadening [2]. For completeness, since the system described in this work is also calibrated with a Californium source, an energy histogram of alpha particles emitted by Californium 252 can be seen in figure 6.4.

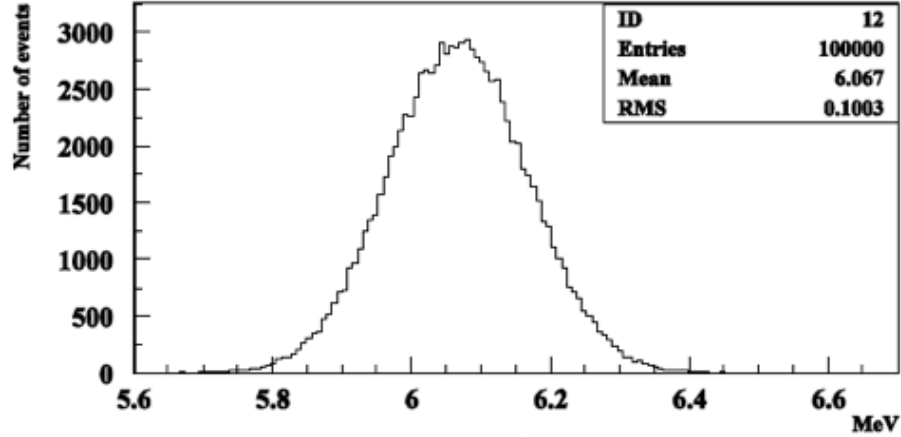


Figure 2.4: Californium 252 main alpha energy spectrum from [3]

2.6.2 Heavy Ion and Fission Fragment Spectroscopy

The energy measurement of fission fragments or other ions of large mass involves several concerns, which are caused by the high density of charge carriers that are created along the particle track. Recombination of electron-hole pairs is accentuated, and the detector may require a higher bias voltage than that which is required to saturate the signal from alpha particles. The need for bias voltage change for the silicon detector used in this work is discussed in section 6.2. The pulse height defect is also accentuated by the higher carrier density complicating the energy measurement procedures. The prolonged exposure to heavy ions or fission fragments creates rapid performance deterioration due to radiation damage to the detector. [2]. The most effective step to minimize pulse height defect and slow rise time is to have as high electric field as possible. Typical measurements of the response function of silicon diodes to monoenergetic heavy ions show an asymmetrical peak with significant tailing toward the low energy side. This is caused by fluctuations in energy loss due to entrance window or in charge lost due to recombination along the particle track. [2] Recording of the fission fragment spectrum from the spontaneously fissioning isotope ^{252}Cf is a standard test of heavy ion detection performance.

Chapter 3

Design of the Front-End Electronics for Radiation Detection

3.1 General Readout Electronics for a Radiation Detector

The fundamental output of all pulse-type radiation detectors, including silicon detectors, is a burst of charge Q liberated by a single radiation quantum in the detector. The charge is proportional to the energy deposited and is delivered in the form of current $I(t)$, where Q is the time integral of the current pulse. The input of the readout electronics is a series of these transient current pulses. These occur at random times with varying time between them and usually with varying amplitudes and durations. The output of the electronics is usually either a count rate or an energy spectrum. An energy spectrum is a measurement of the distribution of energies deposited by the pulses in the detector. [2]

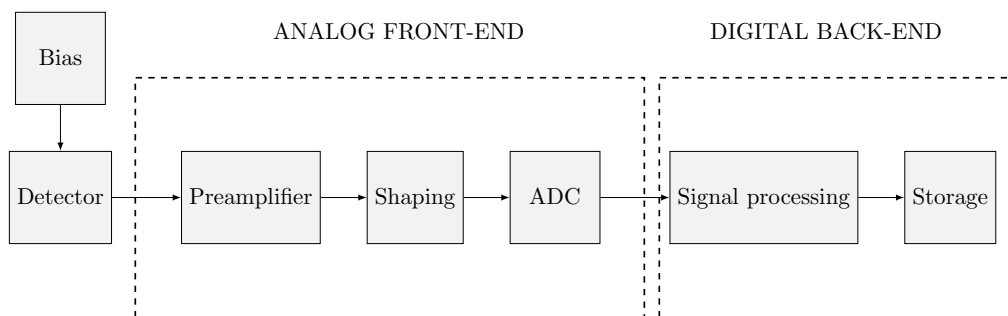


Figure 3.1: Schematic of general electronics for detection of radiation using a silicon detector

Charge-sensitive amplifier, pulse-shaping amplifier and signal processing chains are an essential building block of particle detector front-ends(PDFEs) [16]. The incident particle interacts with the detector which outputs a current pulse. The total charge is too small to be sensed directly. The current from the detector is first sent to a preamplifier, which is an interface between the detector and the subsequent electronics. The preamplifier outputs a voltage step δV proportional to Q . The next step, the shaping stage converts the preamplifier output to a waveform suitable for measurements, producing a voltage pulse with height V_{peak} proportional to the deposited charge. Recording the pulse height and occurrence rate gives us information about the level and charge of the incident radiation. [2]

3.2 Design Considerations for the Front-End Electronics

The front-end electronics have to sometime endure high levels of radiation. This sets additional constraints to the design and implementation. The system should also have a high enough sensitivity and good linearity. The lower bound of radiation detection is set by the noise level. The data readout speed is bounded by the readout and storage systems and how much data they are able to process. [6] Therefore, when designing the front-end electronics both the environment in which the electronics will be used in and the goals of thesis were kept in mind. The main considerations were:

- One of the main goals of the thesis was to design a reasonable alternative to the expensive radiation detection electronics. Therefore, it is best to try to keep the most complex part of the circuit, the ADC, far away from radiation. Radiation effects on silicon ICs are discussed more in section 2.4.2.
- The analog to digital converter operates at a high speed of 125 MHz and outputs single-ended parallel CMOS. Because of this, it is important to keep the ADC close to the FPGA to combat the noisy environment and minimize the skew on the parallel ADC outputs. This is discussed more in section 3.14.
- The FPGA used as the signal readout and processing device is susceptible to single event effect, discussed in 2.4.1, and therefore has to be kept away from radiation sources.
- The preamplifier and the biasing network have to be as close to the detector as possible, to avoid introducing noise to the system, as discussed in section 3.5.
- The environment in which the electronics are to be used are potentially very noisy, for example in the same room as a cyclotron, which produces a great deal of electromagnetic noise, therefore differential signaling should be used in long cables.
- The system should be capable of handling different detectors and have a possibility to connect several detectors at once. Discussion of the general readout electronics for

a thin film breakdown counter are in section 3.12 and for a silicon detector in section 3.1.

With all of the previous kept in mind, it was decided to split the analog front-end into two separate cards. The two cards would be split up so that the components that are more susceptible to radiation induced errors and damage are kept far away from ionizing radiation sources. The card with these components will be referred to as the digital card. As few components as possible are then placed on the first card, which is more exposed to radiation. This card will be referred to as the analog card. Since components exposed to radiation are susceptible to radiation induced error and failure, as discussed in section 2.4.2, the supply current drain is monitored in the first channel of the analog card to detect malfunctions. The general block diagram of the two cards can be seen in figure 3.2.

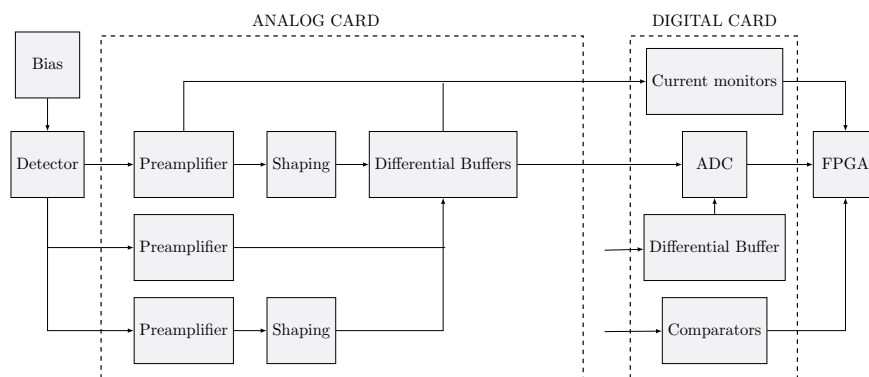


Figure 3.2: Block diagram of the general components of the analog and the digital card

3.3 Analog card

The complete schematic of the analog card can be seen in Appendix A. The analog card has three channels. Two of the channels, channel 1 and 3, are slow channels with pulse shaping, shown in figure 3.4, they have a preamplifier, a shaping amplifier and a differential buffer on them. These channels are designed to output shaped pulses better suited for pulse height discrimination. The shaping amplifier consists of an integrating step and a differentiating step. The design of the shaping step is discussed in more detail in section 3.6.

Channel 2 does not have a shaping step. This channel is meant for timing purposes, as it has a very fast rise time and a small feedback resistor for a short pulse decay time. The preamplifier design is discussed in section 3.5.

Channel 1 on the analog card is set up so that the current of all of the operational amplifiers on it can be monitored through the current monitoring integrated circuits on the digital card. The current monitoring setup is discussed in more detail in section 3.9.

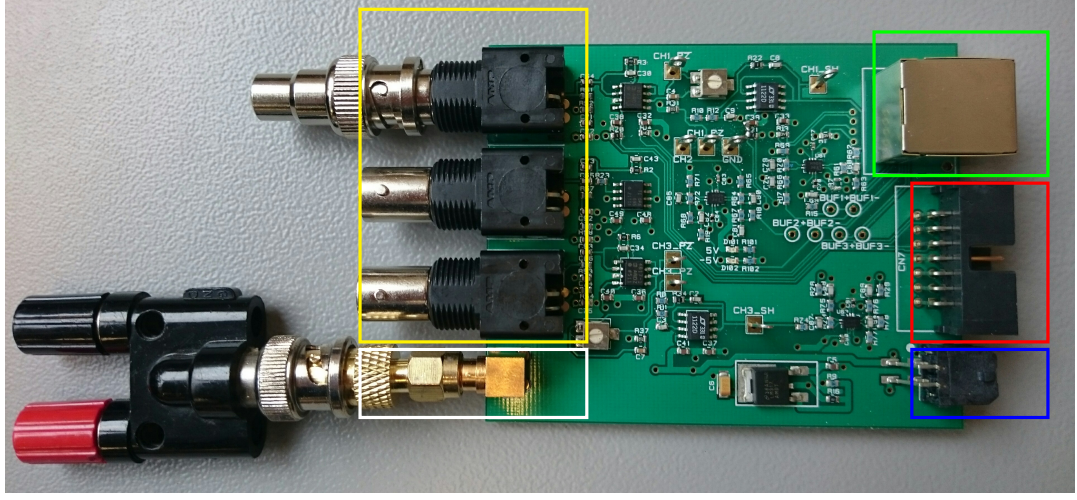


Figure 3.3: Assembled analog card with different connectors marked. Green: RJ45 connector for the differential signal to the digital card, Blue: Power connector for the ± 5 V, White: Bias voltage for the detectors (90 V), Red: Current monitoring connections, Yellow: Inputs for detectors

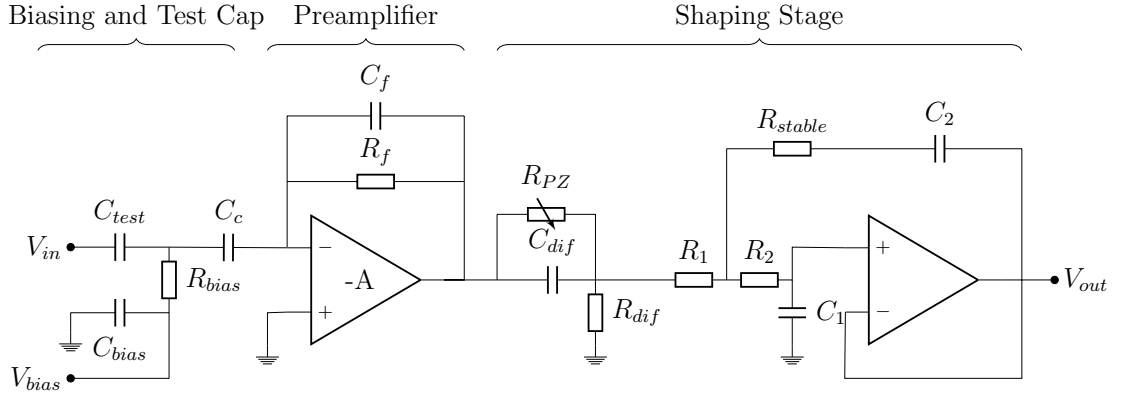


Figure 3.4: Slow channel of the analog card

3.4 Digital card

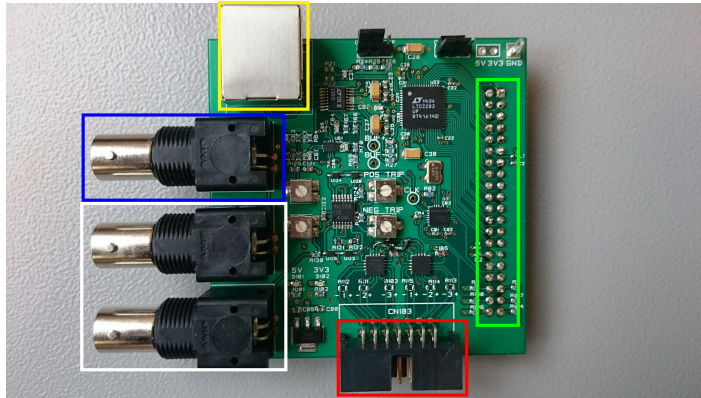


Figure 3.5: Assembled digital card with different connectors marked. Yellow: RJ45 connector for the differential signal from the analog card, Blue: Single-ended input to the on-board differential buffer, White: Digital inputs to the window comparators, Red: Current monitoring connections, Green: Connector to the FPGA (connector on the bottom side of the card)

The digital card consists of 3 major parts:

- ADC and surrounding components which are the on-card differential buffer, the clock generator circuit and the multiplexer in front of channel 2 of the ADC
- The comparator inputs with window comparators
- The two 3-channel shunt current monitors

A block schematic of the digital card can be seen in figure 3.6. The complete schematic of the digital card can be seen in Appendix A.

The ADC Connections

The digital card takes in the output through the RJ45 connector from the analog card and connects channel 1 directly to channel 1A of the ADC. Channel 2 and channel 3 of the analog card are multiplexed together with the on-board differential amplifier to the Channel B of the ADC. The multiplexer is a 4-channel analog differential multiplexer LTC1393 [17] which is controlled using an I2C interface of the FPGA. The clock used by the ADC is generated by the clock generator circuit discussed in section 3.10.

The Comparator (Digital Channel) Connections

The card has two window comparator inputs, which have a voltage divider at the input and are AC-connected to 2.5 V. The inputs can therefore handle both positive and negative pulses. The trigger levels for the window comparators can be set with the help of pot meters. This enables connecting two TFBCs or any other voltage pulse generating detectors directly to the card. The output of the comparators is connected directly to the FPGA for counting. The design of the window comparators is discussed in more detail in chapter 3.13.

The Current Measuring Connections

The third biggest component is the current measuring ICs. These are the INA3221 [4] shunt and bus voltage monitors. The two current monitors have 6 channels between them. The current monitors are controlled using I2C interface of the FPGA. The design and connections of the current monitors are discussed in section 3.9.

Single-Ended Input

It is possible to input a single ended signal, which is then converted to a differential signal by a differential buffer on the digital card. The design of the buffer is described in section 3.7. The output of the differential buffer is connected to one of the inputs of the multiplexer on the card.

Connections to FPGA

The signal map of the connector to the FPGA on the digital card can be found in figure A.2. The connector is plugged directly into the 40 pin header on the FPGA development board. The following signals are connected to the FPGA through the 40-pin header:

- The two output channels of the ADC and the output clock
- the I2C signals to the current monitors, the on-board clock and the multiplexer
- The two outputs from the comparators
- The status signals from the current monitors, these are described in more detail in section 3.9

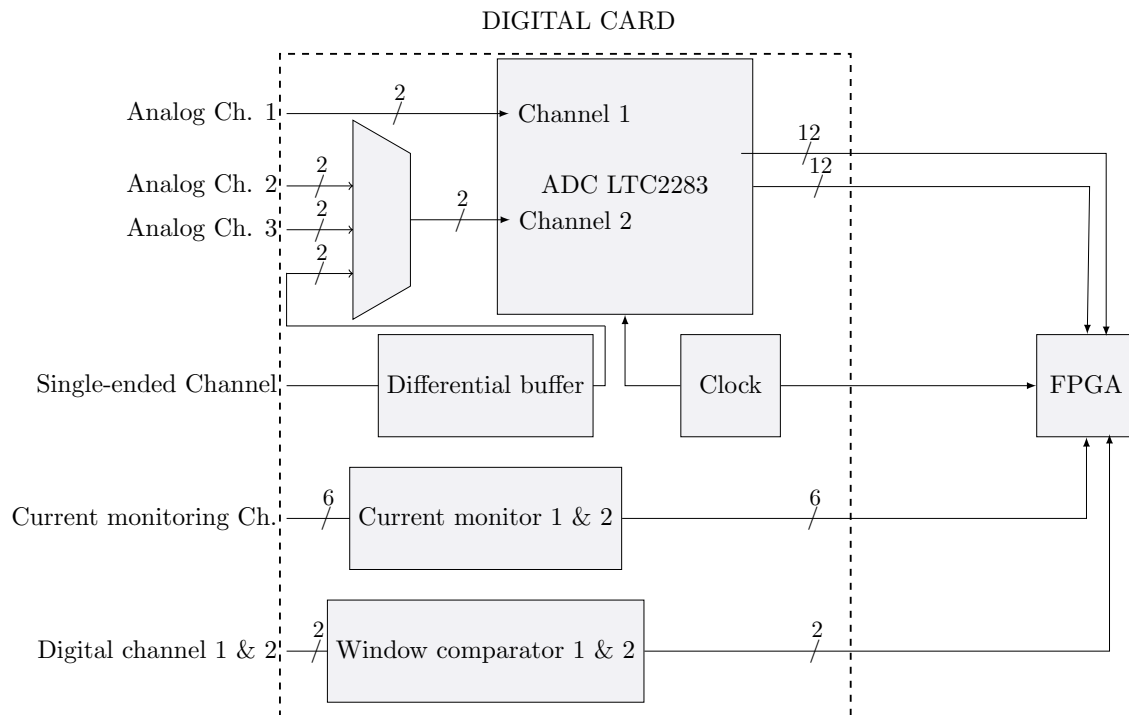


Figure 3.6: The digital card. The number on the connections shows the number of signals.

3.5 Design of the Preamplifier, Biasing Network and Test Input

3.5.1 Preamplifier

The first stage of the front-end electronics is the preamplifier. The preamplifier's main task is to interface the detector with the following shaping and amplifying steps without significantly degrading the intrinsic signal-to-noise ratio. The preamplifier is therefore located as close as possible to the detector. [6]

The three main types of preamplifiers are voltage sensitive, current sensitive and charge sensitive preamplifier, the schematic for all three can be seen in figure 3.7. This work uses the charge sensitive configuration.

The charge-sensitive preamplifier is often preferred over other preamplifiers because it integrates and therefore smooths out the signal. The charge-sensitive preamplifier uses a feedback loop with relatively large resistance R_f and a small capacitance C_f . The input capacitance, including the detector and line capacitance is C_i . The total input capacitance is $C_i + C_f$. The effective input capacitance of the circuit when operating is:

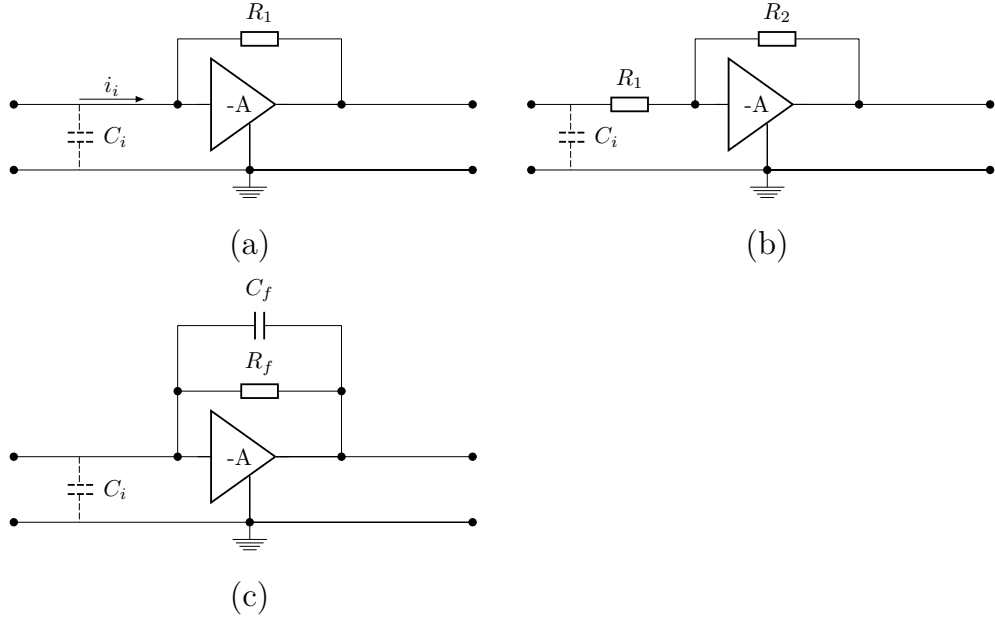


Figure 3.7: Preamplifier configurations: (a) Current-sensitive preamplifier, (b) Voltage-sensitive preamplifier, (c) Charge-sensitive preamplifier

$$C_i + (1 + A)C_f \quad (\text{Miller effect}) \quad (3.1)$$

Assuming R_f is very large the input voltage is:

$$V_i = \frac{Q_i}{C_i + (1 + A)C_f} \quad (3.2)$$

The output voltage is then expressed as:

$$V_o = -AV_i = -A \frac{Q_i}{C_i + (1 + A)C_f} \approx -\frac{Q_i}{C_f} \quad (3.3)$$

This means that the amplitude of the output voltage is virtually independent of the input capacitance and variations in this. [6]. The sensitivity of a detector system using a charge-sensitive preamplifier is defined as:

$$\text{Sensitivity} = \frac{V_o}{E_{det}} \quad (3.4)$$

This is usually expressed in units of mV/MeV. [6]

In order to minimize noise it is essential that the feedback resistance is as large as possible. This is because in a DC state, the feedback capacitor acts as an open circuit, the DC gain is therefore the very high open loop gain. To counter this, a large feedback resistance is inserted in parallel to limit the DC gain to a finite value. Therefore, the changes in the output drift into a finite, small DC error [18]. A very small feedback capacitance, usually around 1 pF is preferred for higher sensitivity as the feedback capacitance. However, the feedback capacitance can not be made arbitrarily small. This is due to both stray capacitances in the circuits board and existing and realizable component values. It should always be sufficiently large compared to any stray capacitances that are unavoidably present in the system. [19]

The decay time of the pulse from the preamplifier is defined by the RC decay constant created by the parallel connection of the feedback capacitance and resistor. The time constant is defined as $\tau = R_f C_f$ and it represents the time the pulse uses to settle down to 36.8% of the baseline from the pulse top. This value is derived from the the equation which represents the voltage in the charging capacitor at any instance of time t, V_0 is the supply voltage: $V(t) = V_0(1 - \exp^{-t/\tau})$ [2].

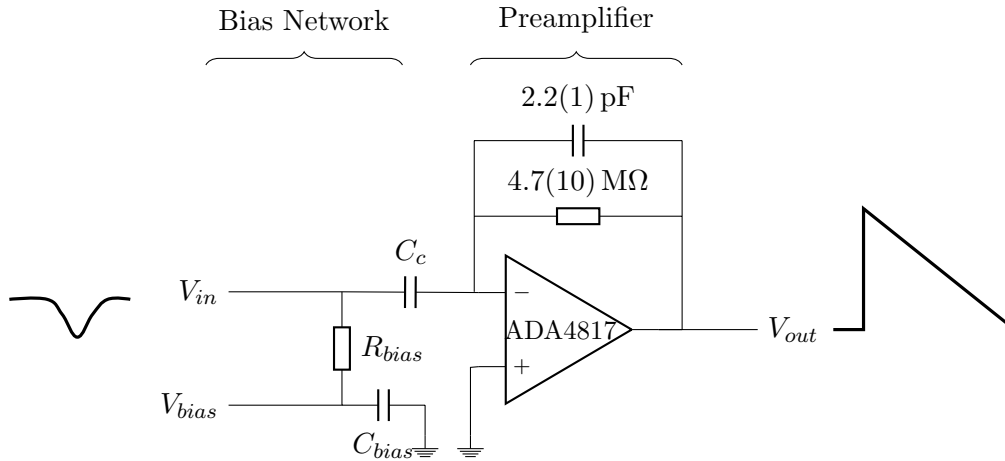


Figure 3.8: Preamplifier ADA4817 with detector bias network, with two tested feedback configurations and typical signal before and after amplification

3.5.2 Choice of the Operational Amplifier for the Preamplifier

The first prototype PCB, which can be seen in figure 3.18, had a somewhat poor choice for a preamplifier, operational amplifier OPA827 [20] was used. Although this is a JFET input operational amplifier with good offset and noise characteristics, the slew rate and bandwidth were not high enough for the application described in this work, as the rise

time of the signal was close to 1 μ s. Therefore, to find the operational amplifier best suited for this work, another PCB was designed and assembled. This PCB, referred to as the analog test PCB, had 3 channels with a total of 3 different operational amplifiers and can be seen in figure 3.18. First, the ADA4817 [21], then the ultra-wideband current feedback operational amplifier OPA695 [22] and finally the fast settling, JFET input LT1122 [23]. The response to test signal for all of these amplifiers was tested. The operational amplifier with the best sensitivity, the ADA4817, was chosen as the final preamplifier for channels 1 and 3 on the analog card. The operational amplifier OPA695 was chosen on the basis of the results in [24]. The paper describes circuit arrangements for current feedback operation amplifiers that allow very fast signals, with rise times down to one nanosecond, while keeping the amplifier stable [24]. The current feedback amplifier requires an additional resistor in the feedback path for stabilization. The operational amplifier was tested with a feedback configuration $R_f = 240 \text{ k}\Omega$ and $C_f = 2.2 \text{ pF}$, which gives a $\tau = 528 \text{ ns}$. The amplifier responded well to the fast settling time and was therefore used in the final design on channel 2, the fast channel. The last operational amplifier, the LT1122 had a somewhat noisy response and was therefore deemed not well suited as a preamplifier, where good noise performance is most critical, as discussed in section 6.1. However, since the amplifier is fast settling and has a good bandwidth, it was used in the shaping amplifier in the integrating stage and works well in that function. Since all of the three operational amplifiers were used in the final design of the analog card, their response to pulses was tested and can be seen in section 5.2.

The operational amplifier used as a preamplifier on channel 1 and 3 in the final design, the ADA4817 [21] is a FastFET, low noise, current feedback amplifier. The amplifier has a slew rate of 870 V/ μ s and a settling time to 0.1% of 9 ns, which is great for high pulse rates. The setup of the preamplifier can be seen in figure 3.8. The final card was tested with feedback resistor values $R_f = 4.7 \text{ M}\Omega$, $C_f = 2.2 \text{ pF}$ and $R_f = 10 \text{ M}\Omega$, $C_f = 1 \text{ pF}$. This gives a pulse decay constants of $\tau = R_f C_f = 2.2 \text{ pF} * 4.7 \text{ M}\Omega = 10.34 \mu\text{s}$ and $\tau = R_f C_f = 1 \text{ pF} * 10 \text{ M}\Omega = 10 \mu\text{s}$. Although the decay time change is minimal, the configuration with $C_f = 1 \text{ pF}$ had a sensitivity that was two times higher, as predicted by equation 3.3. This was therefore the final choice. The choice of the size of the feedback capacitor depends on the energies that one wishes to measure. The linearity and response of both of the operational amplifiers was tested and the results can be seen in section 5.3.

3.5.3 Bias Network

Another function normally carried out by the preamplifier is to provide a means for supply biasing voltage to the detector. The bias network can be seen in figure 3.8. The bias voltage is supplied through a load resistor R_{bias} , which was chosen to be 1 M Ω in this work. This is a typical value used in a bias network. A single cable between the preamplifier and the detector provides then both the bias voltage to the detector and a signal pulse to the input of the preamplifier. The load resistance together with the input capacitance determines

the time constant across which the detector current is collected. Semiconductor diode detectors, such as the one used in this work, are especially prone to leakage currents. When R_{bias} is large, leakage currents can lead to substantial DC voltage drop across the resistor. In this case, the biasing voltage should be raised so that the detector is biased to the correct level. The preamplifier is AC-coupled from the bias voltage by the decoupling capacitor C_c . Care must be taken when increasing the bias voltage as FET input preamplifiers, such as the one used in this work, are prone to over-voltage damage. The preamplifier can be damaged when raising the bias voltage in coarse steps or disconnecting it abruptly. The bias voltage should therefore only be raised gradually. [2]

3.5.4 Test Input

Preamplifiers are often provided with an input labeled test pulse, which receives the output of a pulse generator in order to test the system. [2] The preamplifiers described in this work do not have a test input due to the limited space on the analog card. However, an external test capacitor can be provided and this is how the preamplifier can still be tested. The test capacitance C_{test} can be seen in the schematic of one of the channels of the analog card in figure 3.4.

3.6 Design of the Shaping Stage

The next step after the preamplifier is the shaping stage. The main task of the shaping stage is to convert the pulses from the preamplifier to a pulse form more suitable for measurements. [2] The shaping stage can consist of several stages, usually a differentiation stage with pole/zero cancellation (CR stage) and one or more integrating steps (RC stage). The shaping stage is needed because the output pulses of the preamplifier are so called linear tail pulses, which usually require amplification and filtering to achieve the desired system performance. A shaping stage with both a differentiator and an integrator is referred to as semi-gaussian shaping, because the output signal is close to a gaussian curve. [6] A shaping stage with N differentiating stages and M integrating stages is denoted as $(CR)^N - (RC)^M$. The whole shaping step can be described by a single parameter to define the pulse shaping time, the time constant $\tau = RC$ of the equivalent Semi-Gaussian shaping. Because this single parameter does not clearly define all of the time-related parameters, it is therefore not recommended to not quote this single shaping time. [2] The description of shaping times of all of the shaping stages are discussed in more detail in section 3.6.1.

Noise Considerations of the Shaping Stage

The general noise performance of the system is discussed in more detail in section 5.3.2. In this section, the effect of shaping on the noise performance of the system is discussed.

Since the frequency of the shaped signal is much narrower than of noise, both low- and high pass filtering can be used to reduce the general noise level. If the shaper has a $\tau = 1 \mu\text{s}$, no useful information can be found in the nanosecond range and low-pass filtering removes much of the unwanted high-frequency noise. High-pass filtering can reduce the low-frequency power-line pickup without reducing the integrity of the signal. [2]

As previously mentioned, a system described with the same τ can have different actual shaping times. For example, a $(CR) - (RC)^4$ shaping amplifier with $\tau = 1 \mu\text{s}$ results in a peaking time a factor 4 longer than that of a simple $(CR) - (RC)$ network. If one were to give equal peaking times for the two methods, the more symmetric shape of the Gaussian curve would result in a faster return to the baseline and therefore the pulse pile-up at higher rates is therefore reduced. [2] Therefore, short shaping times are desired to minimize the pulse pile-ups. However, short shaping time carries more wide-band electronic noise and may therefore cause more uncertainty in the pulse height analysis. [2] One can clearly observe the effect of shaping reducing the distortion of pulse height caused by pulse pile-up in figure 3.11.

It can be shown that the best possible signal-to noise ratio is achieved if the signal pulses are shaped to the form of an infinite cusp. In actuality, pulse shape must have finite width, the performance of which can be compared to the infinite cusp. The performance of the infinite cusp is then 1, the performance of a simple CR-RC shaping is 0.736 and the performance of $CR - (RC)^4$ is 0.858. [2] As a compromise between noise and pile-up reduction, the author has chosen the general form $(CR) - (RC)^2$ for the shaping steps. A more thorough description of both the integrating and differentiating steps follows.

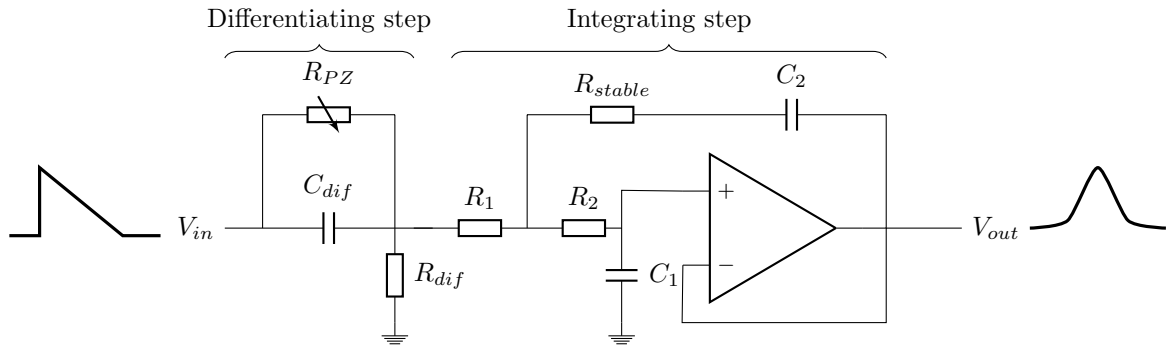


Figure 3.9: Shaping stage with a simple differentiating step and a Sallen-Key integrating step, with typical signal in to and out of the shaping stage

Differentiating (CR) Stage

The general form of the differentiating stage is a capacitor, or an active RC filter, and a pole zero cancellation resistor. The capacitor shortens the output pulse, which causes undershoot in the signal pulse. The principle of the pole/zero cancellation network is that the differentiating step creates a pole defined by the constant $R_{PZ}C_d$ and a zero is created by the preamplifier defined by the feedback components R_fC_f . The cancellation is carried out by changing the value of the variable resistor R_{PZ} until the undershoot disappears. A typical differentiating stage can be seen in figure 3.9. The signal from the differentiating stage with and without the pole/zero cancellation resistor can be seen in figure 3.10.

Integrating (RC) Stage

As was discussed in section 6.1, the pulse shape with a higher number of integrating steps results in a more symmetric Gaussian pulse which returns faster to the baseline. However, since the analog card has 3 shaping channels on it, due to space considerations 2 RC stages were chosen as a compromise between the pile-up reduction, the noise and the space considerations. The integration step of the shaping stage was designed to be a Sallen-Key configuration active filter. A good reason to choose the Sallen-Key configuration for the filter for shaping is its compact design, which provides an active filter with two poles (two RC steps) using one operational amplifier, which means that the two integrating steps can be done with one operational amplifier. Since the operational amplifier is of the current feedback type, a stabilization resistor R_{stable} is needed to prevent the circuit from oscillating. [24] A typical integrating stage can be seen in figure 3.9.

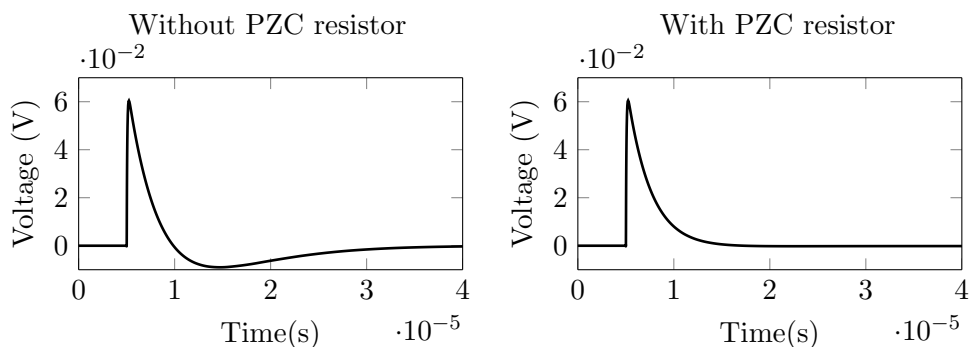


Figure 3.10: LTSpice simulation of a signal after the differentiating step, using the schematic in figure 3.11 with and without pole/zero cancellation resistor

3.6.1 Verification of the Design of the Preamplifier and Shaping Step

A circuit corresponding to the final design of channel 1 and 3 was set up in LTSpice. The schematic of the circuit can be seen in figure 3.11. The values of the components reflect the final design, the operational amplifier used in the simulation is a JFET input amplifier LT1122, which is analogous to the operational amplifier ADA4817 used in the actual design.

The circuit operation was simulated by sending a current pulse equivalent to 1 MeV to the circuit. This was done by sending a step pulse through a test capacitor C_{test} . Charge transfer into the preamplifier is then $Q = V \cdot C_{test}$, where V is the amplitude of the voltage step. The charge equivalent of 1 MeV in silicon was calculated using:

$$1 \text{ MeV(Si)} = (1 \text{ MeV} \times 1.6 \times 10^{-19} \text{ C}/3.6 \text{ eV}) = 0.044 \times 10^{-12} \text{ C} \quad (3.5)$$

where 3.6 eV is the energy per electron-hole pair in silicon [2]. The amplitude of the step into a capacitor with size $C_{test} = 2.2 \text{ pF}$:

$$V = Q/C_{test} = (0.044 \times 10^{-12} \text{ C})/(2.2 \times 10^{-12} \text{ F}) = 20 \text{ mV} \quad (3.6)$$

The 1 nF capacitor and 1 k Ω resistor in the differentiating step gives a fall-time constant of 1 μs . The 1 k Ω resistors and 100 pF resistor in the integrating step give a rise-time constant of 100 ns. The total shaping constant τ of the shaping stage is then $100 \text{ ns} + 1 \mu\text{s} = 1.1 \mu\text{s}$. In the final design of the analog card, the shaping time for the differentiating step has a fall-time constant of 5 μs and the total shaping time was $100 \text{ ns} + 5 \mu\text{s} = 5.1 \mu\text{s}$.

The output of the signals from the preamplifier simulated in LTSpice, after the differentiation step and after the integration step can be seen in figure 3.11. The operation of the shaping stage is visible and the effect of the pulse pile-up is considerable reduced, as was the desired purpose.

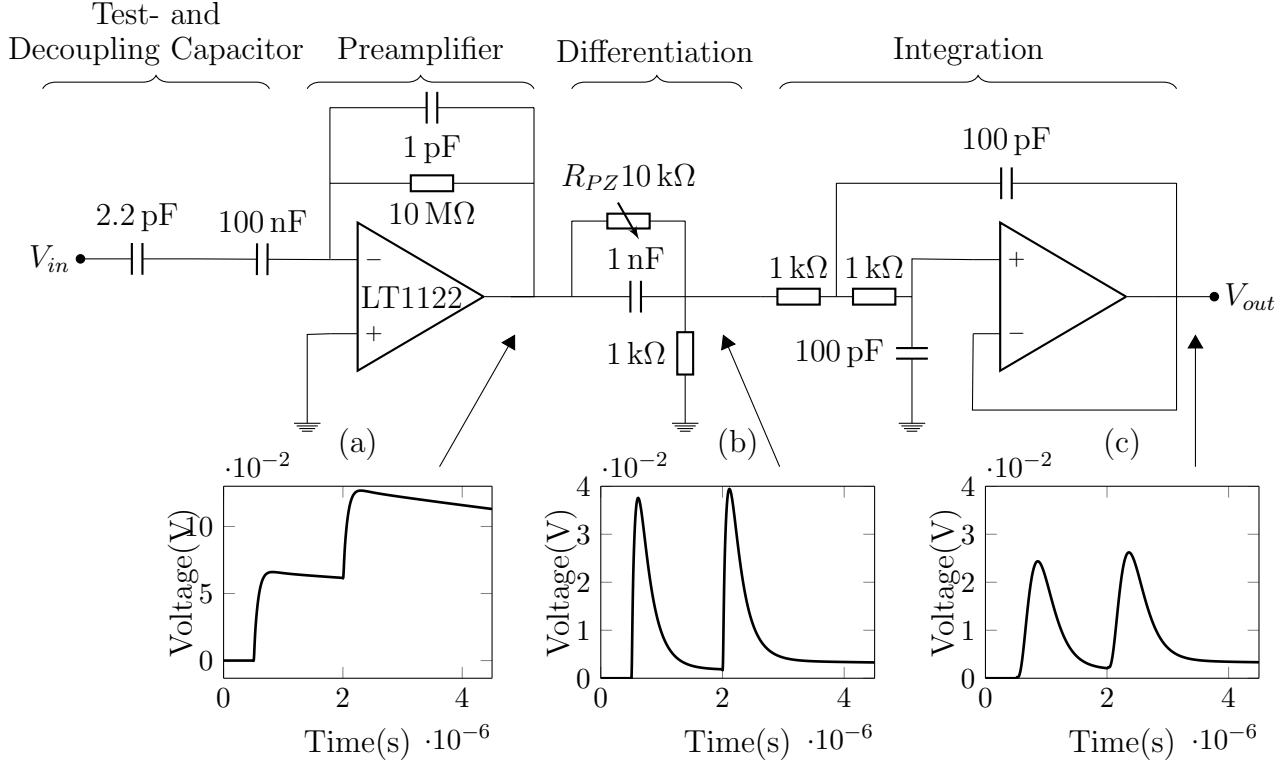


Figure 3.11: Schematic of the test circuit with a preamplifier and shaping stage used in LTSpice. Signal from different stages shown for two 1 MeV equivalent pulses.

3.7 Design of the Differential Buffers

The final step after the shaping stage is the differential buffers, operational amplifier LTC6409 [25]. As the cable between the analog and digital card can be long, it is beneficial to use differential signaling, so that both the positive and negative line are subjected to the same amount of interference. Since the ADC takes in differential signals with common mode of 1.5 V, a logical choice for driving the input was a differential operational amplifier. The amplifier chosen is the very high speed, low distortion LTC6409 [25] differential amplifier with gain bandwidth product of 10 GHz and an input noise density of $1 \text{ nV } \sqrt{\text{Hz}}^{-1}$.

The ADC has a common mode voltage requirement of 1.5 V. This was easily set on the differential buffers by generating a 1.5 V reference on the analog card and supplying the buffers VOCM input with this voltage. On the digital card, the common mode voltage generated by the ADC was used to bias the differential buffer. The gain of the amplifier can be set with external components, the connections of the LTC6409 can be seen in figure

3.12. The component values were set according to the recommendations of the data sheet, the gain was set to 1 V/V for maximum performance on channels with shaping (channel 1 and 3) and 2 V/V for the fast channel (channel 2).

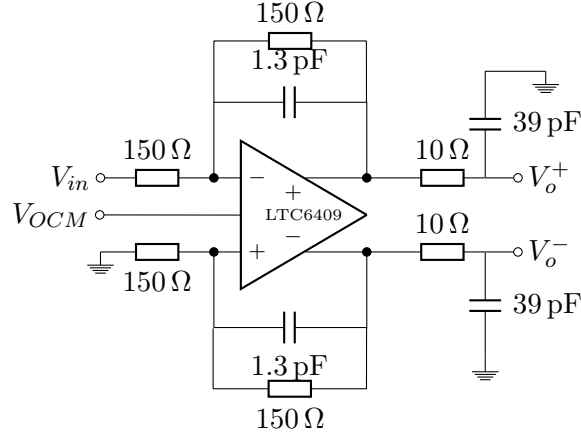


Figure 3.12: Connections of the differential buffer LTC6409 with gain 1 V/V

3.8 Choice of the ADC

3.8.1 Prototype ADC

The ADC for the prototype card was a 250 MSps, 10-bit serial approximation analog to digital converter LTC2242-10 [26]. It was chosen for its speed and a good signal to noise ratio. The encode clock input has to be between 1 MHz and 500 MHz. The outputs can be either CMOS or LVDS. LVDS was chosen as the signaling standard as this type of signal is excellent at high speeds and can be sent over relatively long distances [27]. A longer discussion of the drawbacks and benefits of using either LVDS or CMOS are discussed in section 3.14.

3.8.2 Final design ADC

Although the ADC on the prototype card worked well, due to the need of a large amount of connections for the differential LVDS signals, only one channel could be connected to the FPGA. As one of the goals of the thesis was being able to connect several detectors to the system, a different ADC was chosen. The ADC chosen for the final design is the LTC2283 [28], a 12-bit, 125 MSps, 2-channel serial approximation ADC. The outputs are parallel CMOS. The minimum operating frequency of the ADC is 1 MHz. Although the maximum sampling speed is 125 Msps or 2 times lower than on the prototype ADC, the

speed is adequate for our application. The fast channel of the analog card has a $\tau = 538ns$, this is the fastest signal that needs to be detected and the ADC sampling speed is fast enough for this.

The dual channel ADC has a an analog multiplexer in front of channel B. Figure 3.13 is the representation of connections to channel B of the ADC. The settings of the inputs that can be selected by the designer are listed in table 3.9.

The output buffer of the ADC is powered by the analog voltage OVDD and analog ground OGND which are isolated from the ADC power and ground VDD and GND. The OVDD voltage can be between 3.6 V and 0.6 V, it was chosen to be 2.5 V int his work. The lower the OVDD, the better the signal quality because the output buffers have to drive a smaller signal. Although some FPGAs accept voltage levels down to 1.5 V, 2.5 V is the standard signal level that most FPGAs accept on their general IO pins and was therefor the best choice.

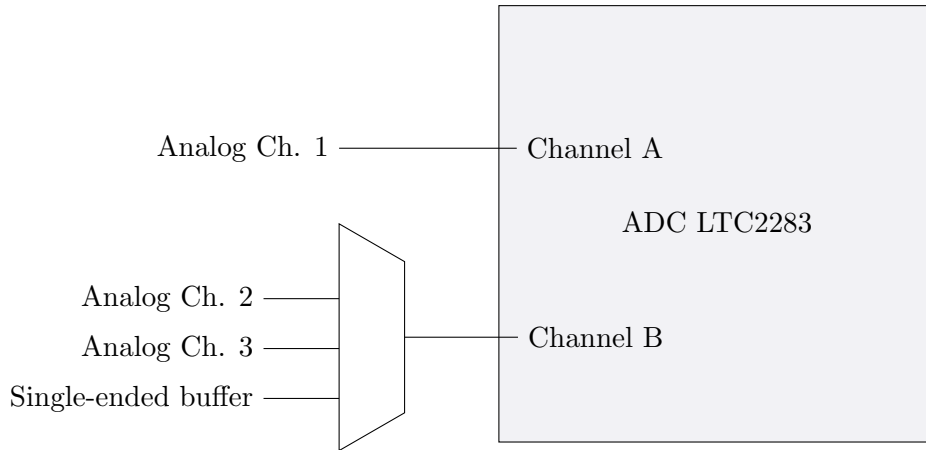


Figure 3.13: The inputs of the ADC LTC2283

Signal	Value (V)	Explanation
SENSE	VDD = 3.3V	Selects the ± 1 V input range and the internal 1.5 V reference
SHDN	VDD or GND	Can be chosen with jumpers on the PCB. VDD sets the output channel to nap mode with outputs at high impedance or GND sets the channel to normal operation
MUX	GND	Channel A signals come out of outputs DB11 to DB0 and Channel B signals come out of outputs DA11 to DA0
MODE	1/3 VDD	Channel Outputs set to offset binary, clock stabilizer circuit on

Table 3.1: ADC LTC2283 settings

3.9 Design of Current Monitoring

The current monitors are the 3-channel shunt and bus monitors INA3221 [4]. The monitors are set up so that it is possible to connect any component to them and measure their current draw. Shunt resistors can be fitted on the PCB, the power supply of the component needs to be connected through the shunt resistor next to the current monitor to measure its current. Care has to be taken that the resistors are of the correct size so the voltage drop over the resistor does not exceed the limit of the monitors, ± 163.8 mV.

The purpose of the current monitoring on the analog card is to observe the effect of radiation on the operational amplifiers on the first channel of the analog card. As the the third channel is analogous the dose is assessed to be similar. As described in section 2.4.2, radiation damage increases standby-current in integrated circuits. By monitoring the current of the operational amplifier, one can verify that they are working correctly. It is also possible to anticipate failure as the standby-current increases rapidly.

Connections of the Current Monitoring Channels

The INA 3221 current monitors can take input voltages from 0 V to 26 V as bus voltage and ± 163.8 mV as shunt. Since the current monitors are high-side, one can monitor the voltage level of the positive input in relation to ground. The typical power supply drain of the ADA4817 ,used as the charge-integrating preamplifier, is 19 mA [21], 7.5 mA for LT1122 [23] used as shaping amplifier and 52 mA for the differential buffer LTC6409 [25]. A shunt resistor value of $R_S = 1 \Omega$ was chosen, which ensures that the shunt voltage remains under the maximum allowed by the monitors and allows for an easy conversion of voltage to current. A typical connection for one of the channels can be seen in figure 3.14. The shunt resistors are located on the analog card on channel 1 on the following IC power

supply lines:

- ADA4817 positive supply
- LT1122 positive supply
- LTC6409 positive supply

In addition to this, it is possible to add shunt resistors on the digital card. This enables monitoring voltage on any component. The connector signal map can be found in figure A.1.

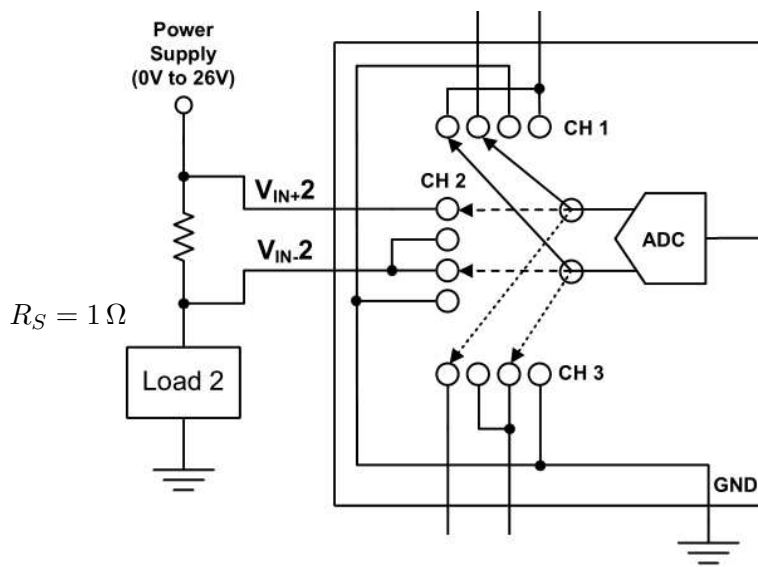


Figure 3.14: Connections of Channel 2 of INA3221 with a shunt resistor R_S . Source: [4]

Warning and Error Signals Generated by the Current Monitors

The current monitors are controlled by the I2C interface from the FPGA. In addition to the I2C connections, the INA3221 outputs 4 alert signals, which are connected to the FPGA, they are: Critical Alert, Warning Alert, Power Valid Alert and Timing Control Alert. The critical alert indicates that the current through the shunt resistor is too high. The warning alert pin is pulled low if any channel exceeds the programmed limit. The power valid alert verifies if all power rails are above the required levels. The power valid level can be set in registers. The timing control is only monitored at power up or after a reset to ensure all

channels are connected to a power source, which is at least 1.2 V [4]. The warning alerts are connected to Leds on the FPGA. Potentially the warning lights could be set up as interrupts to stop data gathering in case of device failure. The setup of the warning signals is the following:

```
LED(0) <= not warn;
LED(1) <= not critical;
LED(2) <= power_valid;
LED(3) <= not timing_control;
```

Controlling the Current Monitors

The current monitors are controlled through the I2C interface of the embedded Linux system on the FPGA. The communication is implemented in a simple C program which reads from and writes to registers on the INA3221. The program is described in more detail in section 4.3.

3.10 Design of clock distribution

The clock circuit chosen in this work is a EEPROM programmable clock generator IDT5V49EE501 [29]. The clock can output two differential clock signals and can be preprogrammed with 6 clock settings and be controlled from the FPGA. During switch-over no glitches occur but there might be frequency or phase shift, depending on the exact phase and frequency relationship between the primary and secondary clocks [29]. The clock generator allows the user to specify the slew rate and loop bandwidth for the four internal PLLs.

The clock provides a sampling clock to the ADC. The data sheet of the ADC specifies that it needs a high quality clock with low jitter and skew, this is because any noise present on the encode signal will result in additional aperture jitter that will be RMS summed with the inherent ADC aperture jitter [28]. The best solution for a reliable, good quality clock distribution is to have a dedicated clock generator on the digital card.

The clock uses an on-board 50 MHz crystal oscillator as a reference. In addition to this, a secondary clock reference from the FPGA can be provided through the external clock input of the IDT5V49EE501. The clock needs to be 3.3V LLVTTL, which can be provided by the FPGA, the input clock frequency has to be between 1MHz and 200 MHz.

The clock generator is controlled using a I2C interface which makes controlling the sampling speed of the ADC easy. The description of the program written to control the clock circuit is in section 4.1.

3.11 Design of the Power Network

3.11.1 Analog Card

The analog card is powered by an external lab power supply which provides $\pm 5\text{ V}$. The card also needs 1.5 V to bias the differential buffers as the ADC needs a differential signal that has a common mode of 1.5 V . This voltage is generated by a positive adjustable DC regulator LM317. The schematic of LM317 connections can be seen in figure 3.15.

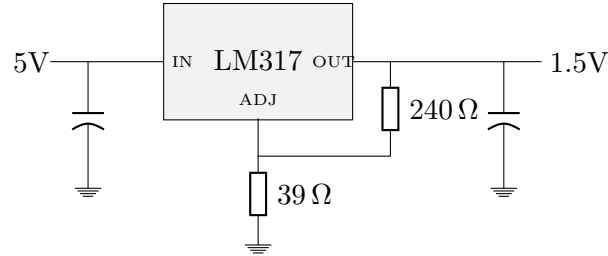


Figure 3.15: Schematic of the connections of the adjustable regulator LM317 to generate 1.5 V

3.11.2 Digital Card

The digital card requires 3.3 V , 5 V and 2.5 V . The first two are provided by the FPGA. The 2.5 V is generated by ADP3338 linear regulator. The FPGA and the digital card power planes have a ferrite bead between them to minimize the high frequency switching noise that is generated by the FPGA. There are also bypass capacitors at the connections to minimize noise.

The digital card has 1 power plane for the 3.3 V , this is the power plane most of the integrated circuits use. The 5 V is used only to generate the 2.5 V . The 2.5 V is the power for the outputs of the ADC. The 3.3 V plane powers the clock generator, the differential buffer LTC6409, the multiplexer, the current monitors and the ADC.

3.12 Readout Electronics for a Thin Film Breakdown Counter

The thin film breakdown counter only needs simple readout electronics. The typical parameters for the signal are: output signal pulse between -1 V and -2 V , duration from 100 ns to 250 ns . This type of detector is used for counting high-energy fission fragments. Thus, only detection of the pulse and not discrimination of its height is required. The typical readout electronics needed to interface the TFBC with an FPGA is simply a biasing network at the input and a comparator to set the discrimination threshold is required. The comparator can then directly be connected to an FPGA as the pulse length of 100 ns is

sufficiently long to be detected by an FPGA with a clock speed, in our case, of 50 MHz. A block schematic for typical readout electronics from a thin film breakdown counter can be seen in figure 3.16.

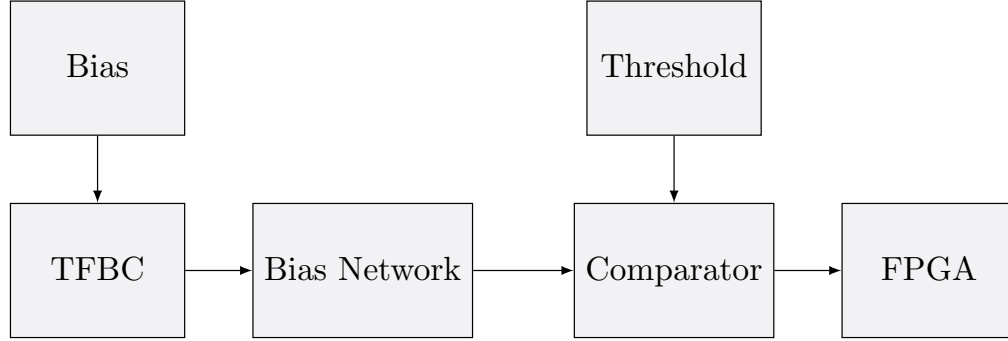


Figure 3.16: Typical readout electronics for a TFBC interfaced with an FPGA

3.13 Window comparator

Comparators are used to set a discrimination threshold voltage for the input signal that is generated by the TFBC counter. To be able to compare both the high and low level of signals, one needs to connect two comparators in a window comparator configuration. The comparator used was the quad low-power MAX9108 [30]. This comparator does not need a pull-up resistor and outputs TTL signals and can therefore directly be interfaced with an FPGA. It also has built-in hysteresis, which makes it useful in a noisy environment. The built-in hysteresis is $2mV$, additional hysteresis can be added with external resistors. The window comparator is configured as shown in figure 3.13.

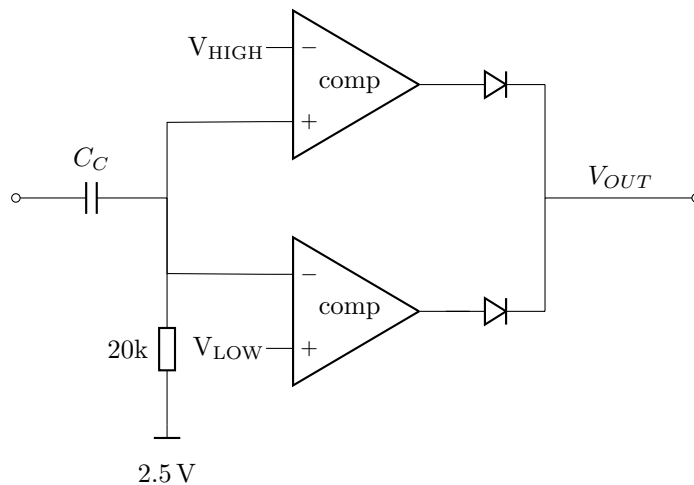


Figure 3.17: Window comparator, with high trigger voltage V_{HIGH} and low trigger voltage V_{LOW}

3.14 Choice between LVDS and CMOS as the signaling standard

3.14.1 Advantages and disadvantages of LVDS

The prototype ADC LTC2242 outputs both CMOS and LVDS, the ADC in the final design LTC2283 outputs only CMOS signals. LVDS signals are defined as having a $\pm 350\text{mV}$ voltage swing and are centered around 1.2V offset voltage. The LVDS signals are differential. The differential receiver rejects common-mode noise from external sources. This is important as the prototype ADC could operate at speeds up to 250 Msps . Good noise performance is necessary to maintain the low voltage swing and controlled edge rates.

The LVDS standard allows very high data rates ranging from 100Mbits/s to over 1Gbit/s/s . The LVDS signals require only simple drivers as only level conversion is necessary on transceiver side [27]. However, LVDS lines are not immune to crosstalk, especially in tracks routed in close proximity. In addition, high speed ADC using LVDS requires more power. In the case of the prototype ADC, the typical power dissipation when in LVDS mode is up to 975mW while in CMOS mode it is typically 740mW [26].

3.14.2 Advantages and disadvantages of CMOS

Single-ended CMOS outputs have longer rise and fall times that limit the maximum bit rate due to the larger voltage swing and are potentially more sensitive to crosstalk and

ground bounce. Ground bounce is a phenomenon where the gate voltage of a transistor can appear to be less than the local ground potential which causes unstable operation of a logic gate. A possible solution for achieving high speeds is using lower output voltage, effectively reducing the CMOS voltage swing. [31]

3.14.3 Final choice of signaling

The first prototype card was chosen to use the LVDS standard to test how fast the system could potentially operate. As the first prototype uses a standard 40 pin rectangular connector, an extension card, THDB-HTG, which converted the HSMC (high speed mezzanine connector) connector on the FPGA to 3 standard 40-pin expansion connectors, had to be used. The LVDS signals were routed on two of the expansion connectors as there are 8 differential receive inputs on the each connector.

A cable was made to connect the 40-pin header on the prototype PCB to the two 40-pin headers on the THDB-HTG expansion card. An alternative to making a cable is having two 40-pin connectors on the card. This is an impractical solution as this option takes a lot of space and makes the PCB unnecessarily large.

The signaling standard for the final design was single-ended CMOS. The PCB with the ADC was moved close to the FPGA to minimize various timing issues associated with high speed signaling over long distances. As CMOS signals can be routed to any of the GPIO pins on the FPGA, only one 40-pin rectangular connector was needed for the final design, despite the final design having two 12 bit channels as opposed to one 10 bit channel on the prototype.

3.15 Layout of the PCB

The digital PCB was designed as a 4-layer card and the analog card was designed as a 2-layer card. Ideally, both of the cards would be 4-layer, as this enables the use of an unbroken ground plane. The advantages of a good ground plane are discussed in section 3.15.4. However, because of the large physical size of the analog card, a 4-layer card was deemed impractical. The large size of the PCB allowed for routing of the signals on just 2 layers, so this was the final choice.

3.15.1 Electromagnetic Compatibility considerations

Wires and current loops on the PCB and in the electric system will act as antennas, emitting electromagnetic radiation that may infer with radio communication and other electric equipment. The same elements of the system will act as receiver antennas for radiation. For good electromagnetic compatibility (EMC) of the design the following basic rules apply [32], all of which were implemented in the design in this thesis:

- Ground plane

- Compact component technology to reduce current loop areas
- Decoupling capacitors where appropriate, this is discussed in more detail in section 3.15.3

Care was taken to ensure that all the analog signals were as far away from the digital outputs as possible. All of the power regulator were also moved to one corner of the card, as they can generate a lot of noise. The input signals were also kept away from the power regulators to avoid causing noise on the inputs.

3.15.2 Differential digital signaling layout considerations

The output signals of the analog card are differential and the differential pairs were therefore routed as close to each-other as possible. This is to minimize the interference from the outside sources so both of the conductors would be exposed to an equal amount of interference. [31] Care was also taken to keep the tracks short and similar length to avoid some of the signals being more delayed.

3.15.3 Bypassing

A bypass capacitor stores an electrical charge that is released to the power line whenever a transient voltage spike occurs. It provides a low-impedance supply, thereby minimizing the noise generated by the switching outputs of the device. It is important to have the bypass capacitors as close as possible to the device that needs the power to avoid drops in the supply voltage. Line inductances can block the charge from the capacitor from flowing, leaving the power line or plane disturbed. [33] All of the power connections to the integrated circuits have 100 nF bypass capacitors as close as possible to the circuit pins on both the analog and digital card.

3.15.4 Ground plane

Both the ADC, the clock generator, the current monitors and the ADC buffer have a thermal pad that has to be connected to a ground plane. In addition to electrical performance, the pad is also important for thermal performance. Most of the heat generated is transferred through the bottom-side exposed pad and package leads onto the printed circuit board. [32]

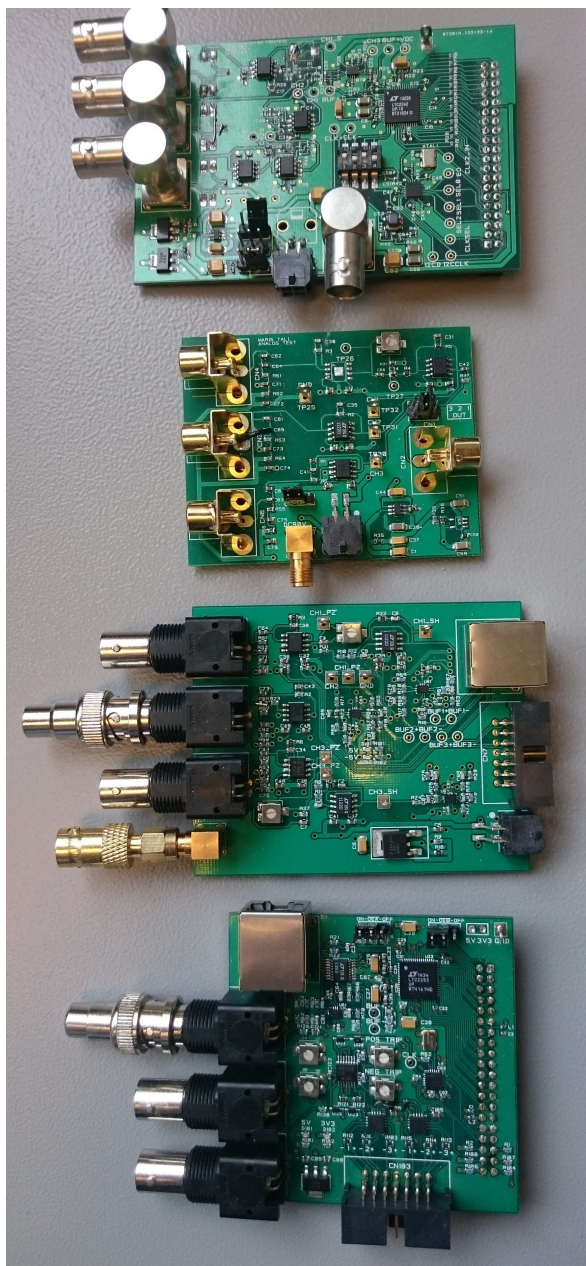


Figure 3.18: All of the PCBs designed and assembled for this thesis. From top to bottom: 1) First prototype, analog and digital parts on the same card 2) Analog test, test for 3 different preamplifiers, 3) Final analog design 4) Final digital design

Chapter 4

Description of the Complete System and Software

4.1 Configuration of the FPGA

The FPGA used for the complete system described in this thesis is the SocKit (rev. D) by Arrow [34].

The whole system for detection of radiation consists of the two electronics cards described in section 3 and a digital back-end solution on an FPGA described in more detail in [5], a block schematic for the complete system can be seen in figure 4.1.

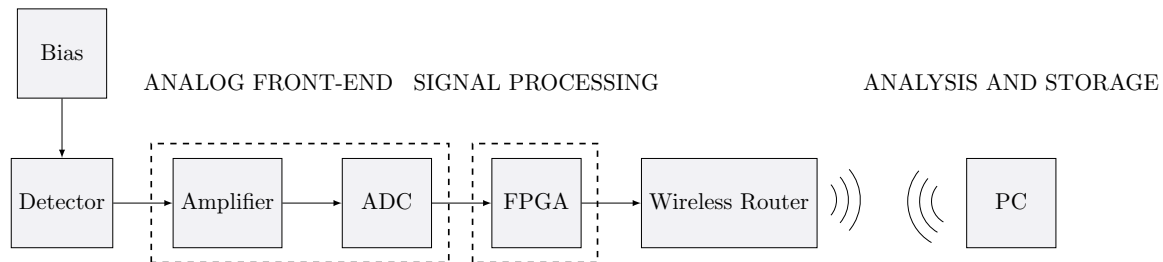


Figure 4.1: Block schematic of the complete system for radiation detection

The digital signal processing system implemented on the FPGA consists on three large modules which are the event trigger, baseline calculation and the zero suppression/pulse height calculation module. The digital signal goes through the following steps to output the processed data [5]:

- The baseline is calculated using a 16 value running average.
- All of the data is buffered through a 5 point event shift register. If all data points

in the event shift register are over the baseline trigger, the baseline calculation is stopped.

- Data is also always buffered through a zero suppression buffer. If the signal goes over the event trigger, the zero suppression module starts writing data to the output buffer
- Pulse height detection is started. Pulse height for the event is calculated relative to the baseline.
- One can choose the amount of padding written to the output data buffer programmatically from the Linux system. This means a number of points before and after an event can be written to the data buffer.
- When the signal falls under the event trigger, the zero suppression buffer stops writing to the output buffer and the pulse height detection stops, the pulse height is written to the pulse height buffer.
- When the signal falls under the baseline trigger level, baseline calculation begins again and the system is ready for a new event

4.2 Embedded Linux on the FPGA

The SocKit includes an integrated ARM processor [34], which has been configured to run an embedded Linux operating system. The FPGA and the Linux system are connected using an Avalon bus. The Avalon bus hardware addresses are mapped to the memory of the Linux system. The addresses can then be opened as files and be read from and written to using the standard Linux read and write commands. The setup and a more detailed description of the system can be read in [5].

The FPGA is connected to a wireless router which enables connecting to the system through Wifi, the static address of the FPGA is 192.168.0.100 and the communication goes through the port 1234. The communication between the software and the embedded Linux on the ARM processor is implemented using a standard socket server written in the C language. The server implementation used is from [35]. The server implementation was modified by the author by implementing threading. The server program allows several clients to connect to it simultaneously but iterates through the received commands concurrently. If one of the tasks sent to the server uses a long time, like data acquisition, the other clients can not send commands to the server program. This was fixed by the author by simplifying sending the function that performs the command interpretation and execution into separate pthreads. This way, the system can simultaneously be accessed by several clients. However, the data from the FPGA can only be read by one client at a time. This is so that the memory is mapped by one thread at a time to avoid concurrency issues with mapping of the Avalon bus by several threads simultaneously.

4.3 Software

4.3.1 Controlling the I2C Peripherals on the Digital Card

The I2C configured using the Qsys program for Altera FPGAs, a more detailed description of the setup can be read in [5]. All the devices on the digital card are connected through the 40-pin header to the FPGA to the I2C bus 0 on the embedded Linux. The pinout of the 40 pin header can be seen in figure A.2.

The devices on the digital card that are connected to the I2C bus 0 with their respective addresses can be seen in table 4.1.

Device	Address	Operations Allowed
Clock IDT5V49EE501	0X6A	Read & Write
Current Monitor 1	0X40	Read & Write
Current Monitor 2	0X41	Read & Write
Multiplexer LTC1393	0X4C	Write

Table 4.1: Devices on the digital card connected to the I2C-0 on the embedded Linux

A short description of the implemented methods for each device follows. Programs to control the multiplexer and two function of the clock program have been included in Appendix B, the basic principles of controlling an I2C devices in the embedded Linux apply for the other devices as well and the programs are therefore not included.

4.3.2 Clock

The clock includes a programming register which is programmed at startup using the configuration saved in the internal EEPROM in the clock IC [29]. The clock is controlled through a C program written by the author which opens the bus I2C-0 as a file and then is written to and read from using the standard Linux read and write commands. The following functionality is implemented in the C program:

- The clock frequency can be programmed with a precision up to 10 kHz. Valid values are set in the program to be from 0 to 125 MHz. If a new ADC is chosen with a higher possible frequency, the C program may be changed to allow setting higher frequencies. The clock circuit itself is capable of outputting clocks with frequencies up to 500 MHz [29].
- Selecting the clock configuration
- Saving the configuration to the EEPROM

- Reloading the configuration from the EEPROM to the program registers
- Shutting down the clock
- Returning the settings of all of the 5 configurations
- Shutting down individual outputs
- Changing the level of the output clock, the choices being 3.3V LVTTL/LVCMOS, LVDS, LVPECL or HCSL
- Writing a programming string generated by the VersaClock 4 software, provided by the manufacturer for easy programming of the clock, to the programming registers of the clock.

The clock program is quite expansive and was not included as a whole this work. Instead, two of the most important methods are included, which are representative for the program. The methods are `set_clock_speed` for setting all of the relevant register values and `calculate_clock_speed` for the actual calculations. The calculation of the clock frequency is done with three nested for loops that compare the target clock speed with the calculated clock speed and only break if the clock speed is accurate to 3 decimal places. This allows for very precise controlling of the sampling speed of the ADC and is important in keeping the amount of uncertainty in the measurements to a minimum. The two functions to control the clock circuit are included in Appendix B.

4.3.3 Current Monitors

The current monitors are controlled through a C program written by the author. The functionality currently implemented in the current monitors is reading out the shunt and bus voltages from all of the outputs.

4.3.4 Multiplexer

The multiplexer is controlled using a C program written by the author. The program enables selecting one of the 4 inputs as the active output or disabling the output. The C program can be seen in Appendix B.

4.4 Main Program to Acquire Data from the System

The program which controls the whole system and gathers informations from the different devices connected to the system was written by the author in Java using the latest Oracle graphical user interface (GUI) application programming interface (API) JavaFX. The program was written in Java for several reasons, the most important being the fact that

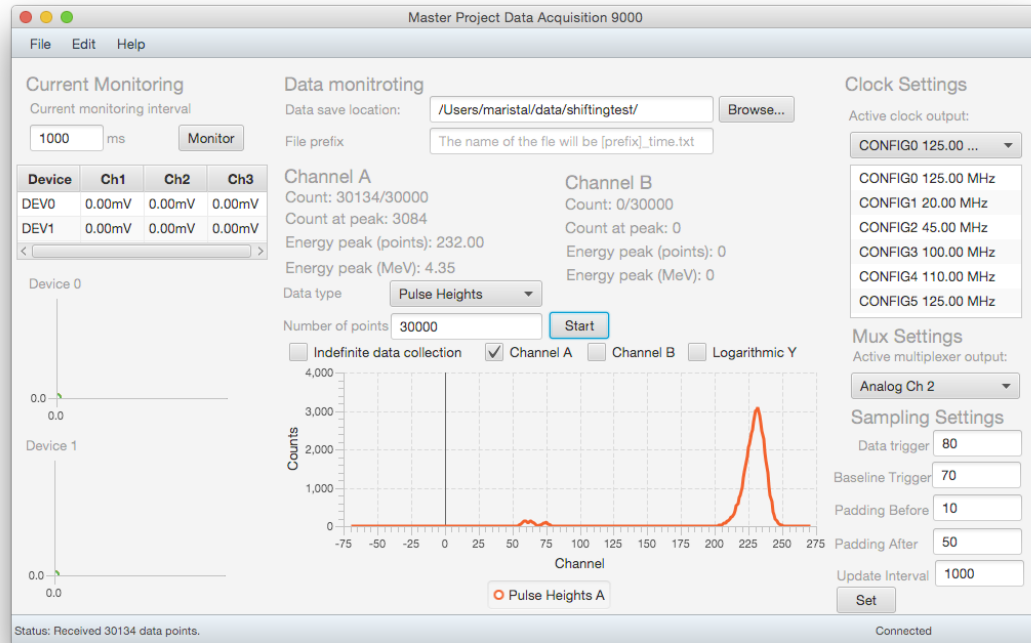


Figure 4.2: The Java program used to control and acquire data from the system described in this thesis

Java programs can be run on any system that has Java installed regardless of the operating system, deploying Java programs is very easy and because Java is such a popular language one can easily find APIs for every imaginable problem. JavaFX was chosen because of all the built-in functionality, where charts were already implemented and all of the GUI runs on threads making the program responsive. The program can be seen in figure 4.2.

The functionality implemented in this program is the following:

- Read out a set number / indefinite number (until Stop is pressed) of pulse heights, pulse heights are saved to a file, location and prefix to the default file name can be chosen
- Read out a set number / indefinite number (until Stop is pressed) of raw pulses, data is saved to a file, location and prefix to the default file name can be chosen.
- The pulse height data is plotted live while it is being gathered, which makes it easy to evaluate results of the measurements right away. Also, one can easily choose to stop the measurement early if something looks incorrect. In addition to this, it is

possible to simply observe the formation of the energy spectrum live and decide when there is enough data in the relevant parts in the spectrum.

- Choose clock configuration
- Choose multiplexer output
- Set the padding for how many points before and after the pulses are saved to the data buffer in the FPGA
- Set the baseline trigger and event trigger
- Monitor the shunt voltages from the current monitors with a chosen interval, this data is saved to a file
- Choose either Channel A or B of the ADC to acquire data from
- Plot the pulse either with a linear or logarithmic Y axis

Chapter 5

Calibration and Testing of the System

5.1 Test equipment and Software Used

5.1.1 Function Generator

The function generator used is the HAMEG 25MHz arbitrary generator HMF2525. The function generator was used in testing the preamplifier and the shaping stages by providing stable negative tail pulses to the circuit. The function generator can also be programmed with an arbitrary waveform. This function was used to simulate pile-ups in the analog circuit.

5.1.2 Power Supply

The power supply used was the HAMEG HMP2020 Programmable power supply. This power supply was used to as a power supply to the analog card and as a test supply for the digital card before connecting the FPGA to it. The power supply allows setting a precise current limit, which was useful in initial setup of the cards. The power supply was set to the expected current draw and if the current draw rose significantly, a fault in the components could be detected and power could be cut instantaneously.

5.1.3 Oscilloscope

The oscilloscope used was the Tektronix DPO2004B Digital Phosphor Oscilloscope with a bandwidth of 70 MHz and maximum sampling speed of 1 GS/s. The probes used were the HAMEG HZ154 probes with variable capacitance. The capacitance of the probes and the oscilloscope outputs were matched using the oscilloscopes PROBE COMP output.

5.1.4 The PCB Design Software

The PCB Design Software used was CadStar Design Editor version 14.0 and 15.0 by Zuken. Both the schematics for the circuit and the PCB layout were performed using this program.

5.1.5 Schematic Simulation

Critical Parts of the circuit were simulated using LTSpiceIV version 4.20.

5.1.6 Data Analyzing and Plotting

The data was analyzed using MATLAB R2014b, both the 64-bit Windows version and the 64-bit OS X version.

5.2 Testing the analog card

5.2.1 Test setup for the analog card

The test setup for the analog card consists of a laboratory powers supply to supply the $\pm 5\text{ V}$ for the card, a signal generator to generate test pulses and an oscilloscope. The analog card has a test capacitor discussed in section 3.5.4 on channel 2, the other channels need an external test capacitor. The test was performed by sending stable negative tail pulses from the signal generator to the amplifier and observing the output. The amplitude of the voltage pulse needed to simulate 1 MeV of charge in silicon is described in equation 3.6. The amplitude of the voltage signal through a 1 pF capacitor was calculated to be 44 mV.

5.2.2 Testing the preamplifier and shaping stage

Channel 1 and Channel 3

Channels 1 and 3 have shaping and are referred to as slow channels. The preamplifier ADA4817 has a feedback resistor of $10\text{ M}\Omega$ and a feedback capacitor of 1 pF, which gives a preamplifier time constant of $10\text{ }\mu\text{s}$. The output of the preamplifier with a test signal with an amplitude of 44 mV through a 1 pF capacitor, which is the equivalent of 1 MeV of charge, gives the output seen in figure 5.1.

The output after the preamplifier is marked signal a, after the differentiating stage is marked signal b and the output of the integrating stage as signal c in figure 5.1. The 1 nF capacitor and $5\text{ k}\Omega$ resistor in the differentiating step give a fall-time constant of $5\text{ }\mu\text{s}$. The $1\text{ k}\Omega$ resistors and 100 pF resistor in the integrating step give a rise-time constant of 100 ns. The total shaping constant τ of the shaping stage is then $100\text{ ns} + 5\text{ }\mu\text{s} = 5.1\text{ }\mu\text{s}$. The test shows that the theoretical values correspond well with the actual measured values.

The sensitivity of the stages to a 1 MeV is was measured to be as follows:

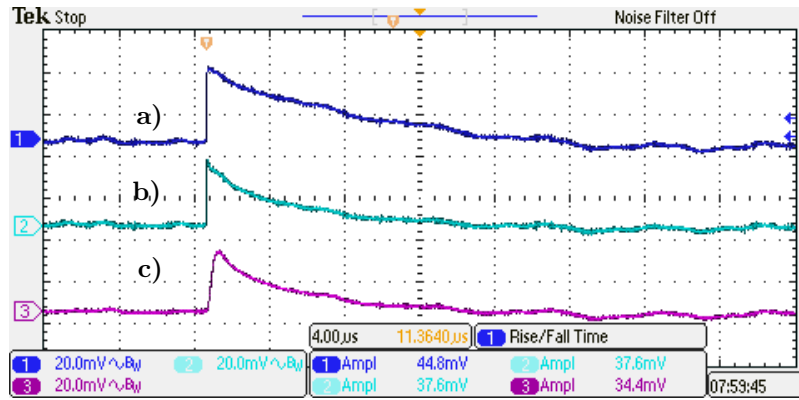


Figure 5.1: Response of the preamplifier and shaping stage to a 1 MeV charge equivalent. a) signal after preamplifier, b) after the differentiating stage, c) after integrating stage

- The preamplifier has a sensitivity of about 45 mV/MeV
- After the differentiating stage, the sensitivity was about 37 mV/MeV
- After the integrating stage, the sensitivity was about 34 mV/MeV
- After the differential buffer with gain $G = 1$, the sensitivity was about 24 mV/MeV

The total sensitivity of channel 1 is the sensitivity measured at the differential buffer, 24 mV/MeV. The total attenuation of the signal on the analog card from the preamplifier to the differential buffer is therefore $24 \text{ mV} / 45 \text{ mV} = 0.5$ or $20 \cdot \log(24 \text{ mV} / 45 \text{ mV}) = -5.46 \text{ dB}$.

The maximum input signal pulse that can be sent into the preamplifier without clipping was tested and was found to be 5.144 V through a 1 pF test capacitor, which is equivalent to $5.144 \text{ V} / 44 \text{ mV} = 116.9091 \text{ MeV}$.

Channel 2

Channel 2 does not have shaping and is referred to as the fast channel. The current feedback preamplifier OPA695 has a feedback resistor of 180 k Ω and feedback capacitance of 1 pF, this gives a fall time constant of 180 ns. The output of the preamplifier and differential buffer to a 1 MeV charge equivalent can be seen in figure 5.2.

- Sensitivity of the fast preamplifier is 15 mV/MeV
- Sensitivity of the differential buffer with gain $G = 2$ is 19 mV/MeV

The total sensitivity of channel 2 is the sensitivity measured at the differential buffer, 19 mV/MeV. The amplification of the signal through channel 2 is therefore $19 \text{ mV} / 15 \text{ mV} = 1.3$ or $20 \cdot \log(19 \text{ mV} / 15 \text{ mV}) = 2 \text{ dB}$.

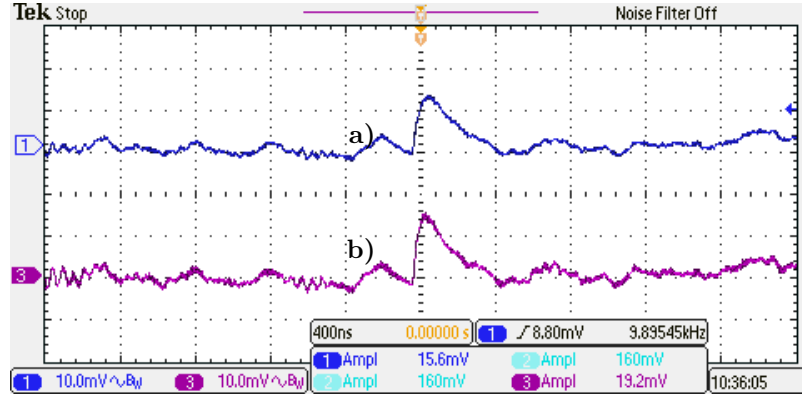


Figure 5.2: Response of the fast channel, channel 2, preamplifier and differential buffer with gain $G = 2$ to a 1 MeV charge equivalent. a) signal from preamplifier b) signal from differential buffer (AC connected to probe, + output)

5.3 Testing of the complete system

The complete system was tested by connecting a signal source through a test capacitor to a channel to be tested on the analog card, connecting the analog card to the digital card and using the software described in section 4.3 to read out data from the FPGA.

5.3.1 Test of Linearity of the System and Energy Calibration

The ideal system would perform a perfect conversion of pulse height to channel number. This is however not the situation in real systems and the amount of nonlinearity of the system needs to be measured. A pulse generator can be used to generate pulses of known amplitude. The most straightforward method to measure nonlinearity is to make a plot of pulse amplitude versus channel number. The maximum deviation of the measured curve from the linear fit is called the integral nonlinearity and is given as a percentage of the full range of the system [2].

The linearity of both channel 1 and channel 2 on the analog card were measured, channel 1 and 3 are identical. As the calibration is dependent on the baseline trigger level, as described in section 5.3.1, channel 1 was tested with both trigger levels 20 and 40. As channel 2 will only be used for timing purposes, it was measured only with trigger level 20.

The test of linearity was performed by sending pulses from a signal generator to the input of the preamplifier, and shaping stage to the ADC and the pulse heights were read out from the FPGA. Then using the Java program designed for the system in this work to count 100000 pulses and recording the bin value with the highest count, the response of the system was found. Equation 3.6 describes the calculation of equivalent charge when a voltage pulse is sent through a test capacitor. The resulting response was plotted and

the linear fit was found using the polyfit function in MATLAB, which estimates the least squares first degree (linear) fit. The linear fit is used as a calibration equation to convert the data from the ADC to the equivalent energy in MeV. The linear fit can be seen in figure 5.3 for the system in the first configuration. The integral linearity calculated on the basis of these fits is also given in table 5.2. All of the results of the linearity measurement can be seen in table 5.1. The trigger level referred to in this table is the baseline trigger level, described in more detail in section 4.1.

Value (equivalent charge)	Channel 1 (trigger 20)	Channel 1 (trigger 40)	Channel 2 (trigger 20)
1 MeV	66	-	72
2 MeV	160	-	133
5 MeV	286	271	322
10 MeV	558	545	637
15 MeV	-	815	-
20 MeV	1180	1085	1265
30 MeV	1652	1622	1896
32.25 MeV	-	-	2043
40 MeV	2039	2029	over maximum

Table 5.1: Measurements obtained during the calibrations of the channels, baseline trigger level 20

The linear fit was calculated without the point at 40 MeV, as described in [2] the edge cases are often nonlinear. The linear fit has the form $y(x) = x*p1 + p2$, where y is the charge in MeV and x is the pulse height in offset binary points from the ADC. The goodness of the linear fit was evaluated by finding the coefficient of determination or R squared value, which is defined as the residual variance from the fit. This value indicates how closely values obtained from the fitting match the data. R squared has values from 0 to 1, 1 being a perfect fit. The R squared value was found using the following MATLAB code, found on the MATLAB central Documentation [36]. Here x and y are the data from the calibration.

```
p = polyfit(x, y, 1);
yfit = x*p(1) + p(2);
yresid = y - yfit;
SSresid = sum(yresid.^2);
SStotal = (length(y1)-1) * var(y1);
rsq = 1 - SSresid/SStotal
```

The R squared value for channel 1 was found to be $R^2 = 0.9972$ and $R^2 = 1.00$ for the channel 2. This means that the linear fit or the calibration equation predicts 99.72% of the variance for the channel 1 and 100% of the variance for the channel 2. The very good performance of channel 2 is due to it having a test capacitor on the actual PCB, while channel 1 was tested with an external test capacitor. These values show however that both channels show a very high degree of linearity and the nonlinearity of the system from purely electronics should not affect energy measurements by any discernible amount.

With the linear fit equation we can also calculate the limits of the system by finding $y(0)$ and $y(2048)$ (maximum pulse height). The lower limit is $y(p2) = 0$ MeV and $y(2048)$. The theoretical resolution of the ADC in MeV can be found by calculating the difference between two arbitrary points from the ADC, for example $y(101) - y(100)$. Both the actual resolution of the system and the lowest detectable value is limited by both the electronic noise inherent to the system and background the noise generated by the detector, which is discussed in more detail in section 5.3.2. The values calculated from all of the channels can be seen in table 5.2. The trigger referred to in this table is the baseline trigger level.

Value	Channel 1 (trigger 20)	Channel 2 (trigger 20)
Fit Equation	$y(x) = x * 0.018 - 0.44$	$y(x) = x * 0.016 - 0.12$
Maximum Value (MeV)	$y(2048) = 36.42$ MeV	$y(2048) = 32.6$ MeV
Minimum Value, 0 MeV (ADC data points)	$x(0) = 24.4$	$x(0) = 7.5$
Resolution of the ADC	18 keV	16 keV
Integral Nonlinearity	$52/4096 = 1.27\%$	$4/4096 = 0.1\%$
Value	Channel 1 (trigger 40)	-
Fit Equation	$y(x) = x * 0.019 - 0.065$	-
Maximum Value (MeV)	$y(2048) = 38.84$ MeV	-
Minimum Value, 0 MeV (ADC data points)	$x(0) = 3.42$	-
Resolution of the ADC	19 keV	-
Integral Nonlinearity	$52/4096 = 1.27\%$	-

Table 5.2: Theoretical properties of the system calculated from the calibration equations

The Shifting of Pulse Heights

As discussed in the description of the system in section 4.1, the baseline calculation is controlled by the baseline trigger. Because of the finite speed of the sampling, any one

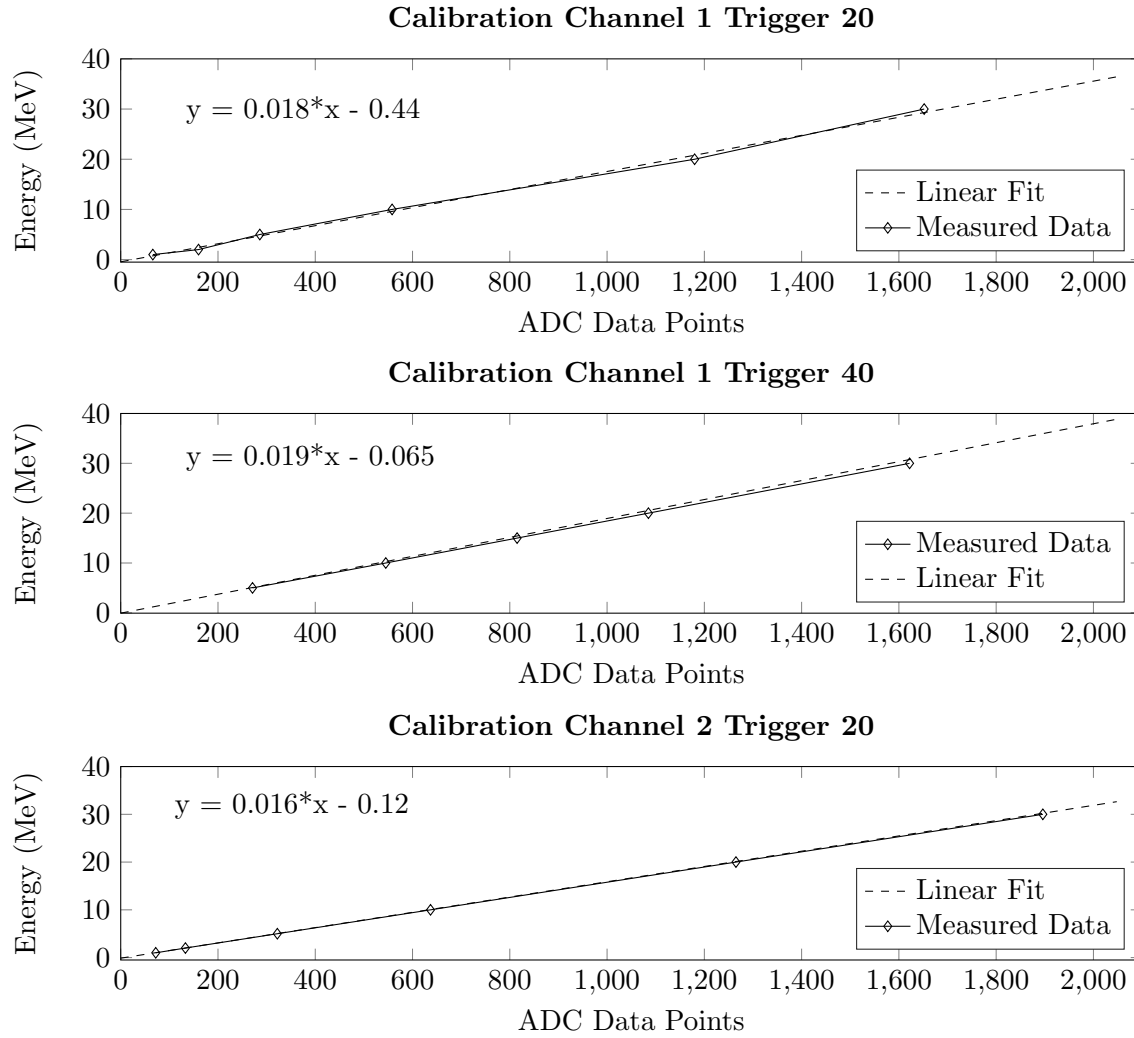


Figure 5.3: Test of linearity for channel 1 and channel 2, with trigger level 20 and channel 1 with trigger level 40

event consists of a limited number of points. By changing the baseline trigger value, one also changes how much of the signal is included in the baseline calculation. If the charge into the system is small, the rising edge of the event pulse consists of a lower number of points. If the baseline trigger level is set too high, the baseline returned by the FPGA is not correct. If the baseline trigger is lower than the noise level, the baseline is calculated incorrectly and starts to drift. Therefore, the baseline trigger level has to be set over the noise level but not so high as to eat away the signal. During the linearity calibration, the noise level of the system was low and the baseline trigger level was set to 20 points. However, during the actual testing with a radioactive source the overall noise level increased, as discussed in section 5.3.2 and the trigger level needed to be set higher. The change in the pulse heights due to change in the baseline was measured by reading 10 000 pulse heights and recording the center channel of the pulse height spectrum. The results can be seen in table 5.3.

Baseline trigger	Channel (shift) 2 MeV	Channel (shift) 5 MeV	Channel (shift) 10 MeV
5	121 (0)	280 (0)	543 (0)
10	119 (2)	278 (2)	541 (2)
20	115 (6)	274 (6)	540 (3)
30	102 (19)	273 (7)	538 (5)
40	-	266 (14)	537 (6)
50	-	260 (20)	534 (9)

Table 5.3: Measurements obtained during the pulse height shifting calibration, values in ADC data points

We can see in figure 5.4, as predicted, the shift is less significant for higher pulses because they contain more data points. However, for lower pulse heights, the shift becomes significant at higher baseline trigger levels. Therefore, it is important that the calibration of the system and the measurements are performed with the same trigger level. Since the shift is not linear and correction is therefore not straightforward, the best strategy is to calibrate for a certain baseline trigger level and use this for all measurements. The system has been calibrated for both trigger levels 20 and 40 on channel 1 and 20 for channel 2.

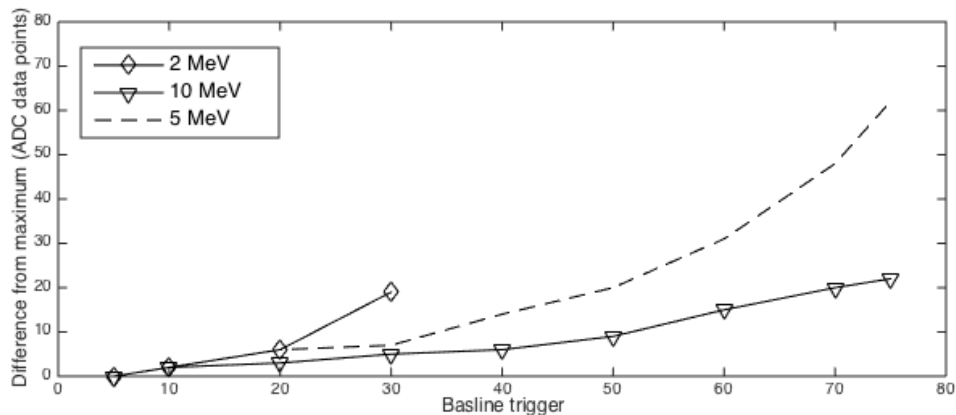


Figure 5.4: The shift in pulse heights when different baseline trigger levels are used

5.3.2 Noise of the System

Sources of electronic noise in spectroscopic measurements can be divided into two categories: series noise and parallel noise. For silicon detectors three main components to the electronic noise are most significant:

- Fluctuations in the bulk generated leakage current, a component of parallel noise
- Fluctuations in the surface leakage current, parallel noise
- Noise associated with series resistance or poor electrical contacts to the detector, series noise

The relative importance of these sources depends on the magnitude of the leakage currents for the specific detector, the capacitance of the detector and whether the diode is partially or fully depleted. [2]

Noise can generally be divided into interference noise and inherent noise. Interference noise is the result of unwanted interactions between the circuit and the outside world or between parts of the circuit itself. A good example of this is power supply noise on ground wires on 50 Hz, or clock feed-through or microphonics noise discussed in the following section. Interference noise can be minimized with careful circuit layout and wiring. In contrast, inherent noise can be reduced but never eliminated since this noise is due to fundamental properties of circuits. This type of noise is thermal, shot and flicker noise. Therefore, when analyzing noise, one must assume that there is some noise present in all possible frequencies. [18] Noise considerations when designing the shaping stage of the system are discussed in section 6.1

Frequency-domain techniques are useful when dealing with random signals such as noise. Periodic signals have power at distinct frequency locations, random signals have their

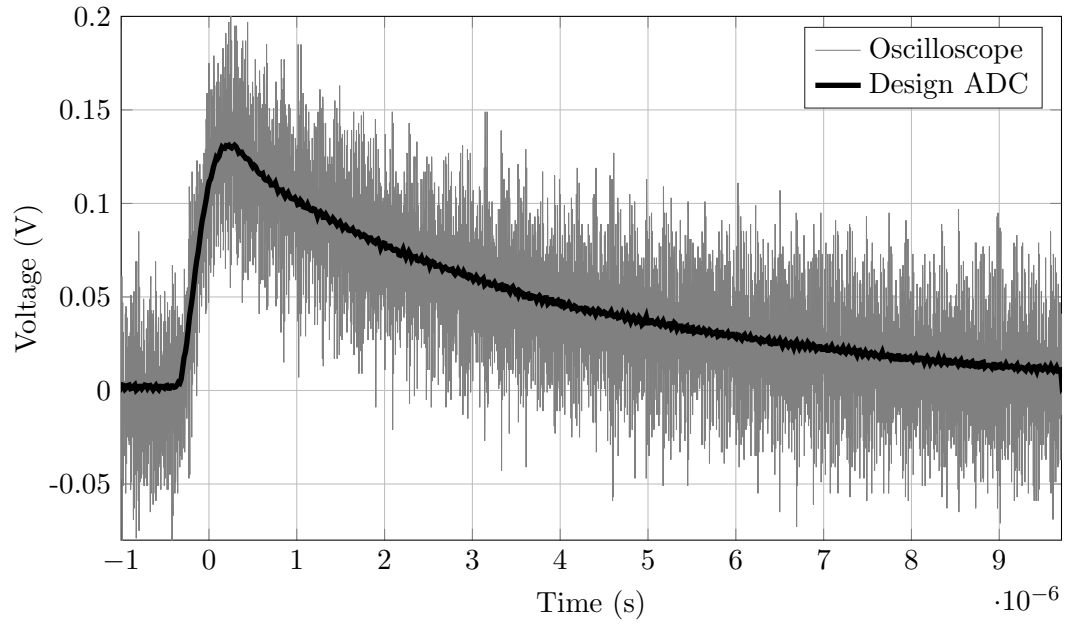


Figure 5.5: Example of inherent noise on top of a signal with equivalent charge of 10MeV sampled with 2.5GSps with an oscilloscope and with 125MSps with the system described in this thesis.

power spread over the frequency spectrum. Mean-squared value of a random noise signal at one single precise frequency is zero. Since the mean-squared value obtained is proportional to the resolution bandwidth, the value has to be normalized to 1 Hz. The frequency-domain representation of a noise signal is its spectral density: the average normalized power that may be measured within a 1 Hz bandwidth. [18]

One has to take into consideration that the ADC has a sampling speed of $F_s = 125$ MHz. The sampling theorem says that for unique correspondence of between an analog signal and the digital version reconstructed from its samples, the sampling rate must exceed twice the highest sampling frequency. The value $S = 2f_{max}$ is called the critical sampling rate or Nyquist rate. [37]

Since by definition noise is found in all frequencies, the maximum frequency of the noise we can detect by sampling with the ADC is $F_s/2 = 62.5$ MHz. All of the noise on higher frequencies will be folded back into frequencies we can sample. [37] A good illustration of this point can be seen in figure 5.5, where the inherent noise of the system is well visible when sampled with higher speeds.

Noise Contribution of the Silicon Detector

To assess the noise spectral density of the system with and without the detector, the output of the slow channel, channel 1, was read with the zero cancellation and the pulse height correction modules turned off on the FPGA. 1000000 points of raw data were read using the FPGA with the detector connected to the analog card and then the same number of points with the detector disconnected from the analog card. The power spectral density for both of these data was calculated using MATLAB. The noise power spectral density was found using the periodogram function in MATLAB. The following code plots the power spectral density of the signal x sampled with frequency F_s in units of db/Hz . This is useful when dealing with signals from the ADC which are offset binary and therefore unitless:

```
periodogram(x,rectwin(length(x)),length(x),Fs)
```

The power spectral density plotted up to 20 MHz with the absolute difference between the two spectral densities can be seen in figure 5.6. The calculated absolute difference was smoothed using a 1000 points moving average, which corresponds to 1 kHz to make the data easier to read. One can clearly see that the detector increases the noise density, especially at lower frequencies. The difference at DC level is 38 dB but decreases as the frequency goes up and then flattens and remains about 10 dB higher at higher frequencies.

Another type of noise caused by the detector called microphonics can be a problem in practical detector systems. Mechanical vibrations transmitted the detector-preamplifier input stage can produce small fluctuations in capacitance that cause a modulation of the output signal. The effects are most pronounced in systems in which a small charge per pulse requires keeping the input stage capacitance at a minimum, such as a silicon detector. It has been demonstrated that a capacitance change of only 5×10^{-7} pF between the FET

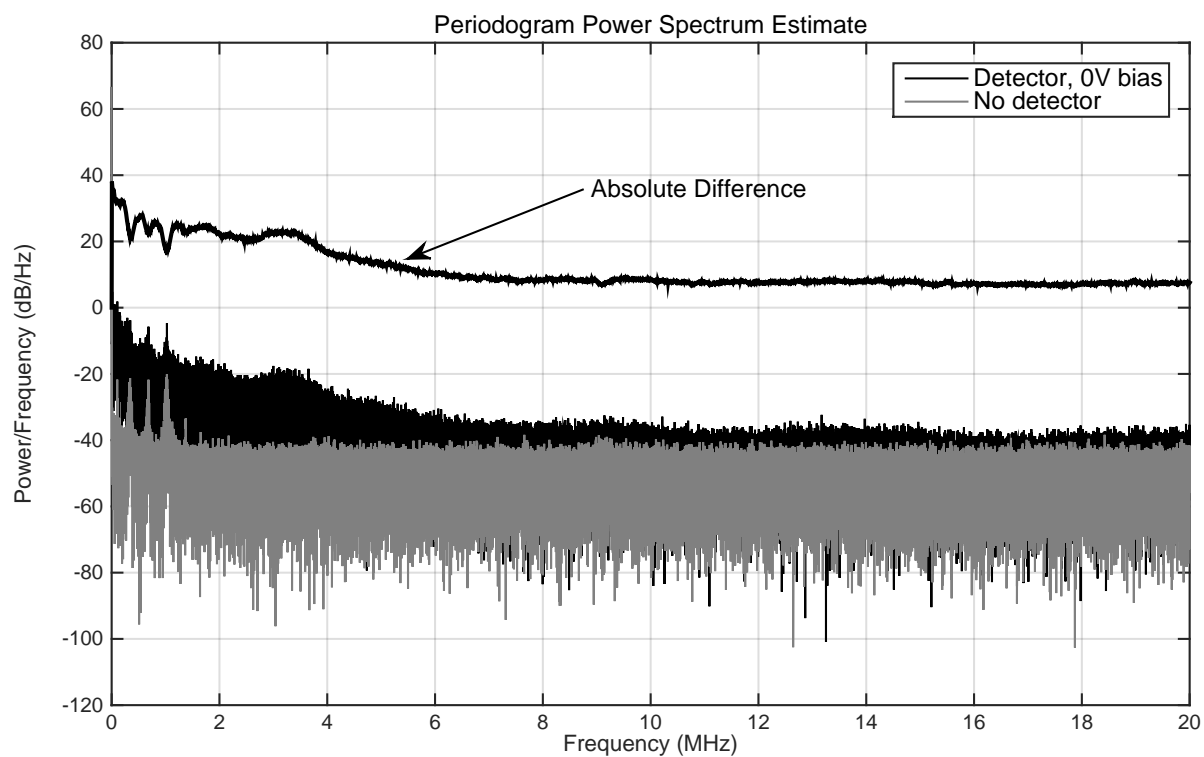


Figure 5.6: The power spectral density from data acquired from the analog card with the averaged difference between the two signals, plotted up to 20 MHz to demonstrate the effect of connecting the detector on lower frequency noise

gate and the high voltage bias of a Si(Li) system corresponds to a microphonic signal equivalent to the deposition of a charge of 10 eV. [2] This effect was observed in practice by the author when placing sources on the detector. A small knock on the plate on top of the silicon detector could produce voltage pulses equivalent to more than 5 MeV. It is therefore imperative that the detector and the analog front end are in a stable environment when conducting testing.

Electronic Noise of the System

The electronic noise is a type of inherent noise, which can be reduced but not removed completely. The electronic noise contribution to the total system noise can be found by sending test pulses with a constant amplitude through the system and recording the full width at half maximum (FWHM) value of the resulting energy histogram. [2] FWHM is equal to 2.35 standard deviations of the histogram produced [2], the electronic noise is considered normally distributed in a system. The test of the electric noise of the slow channel, channel 1, with $C_f = 1$ pF was conducted by sending the equivalent of 1 MeV charge to the preamplifier by sending tail pulses through a capacitor. Equation 3.6 was used to calculate the required amplitude of the test pulses.

When measuring the electronic noise of the system, care has to be taken not to introduce unwanted sources of noise to the system. Probing the analog card while reading out test pulses considerably worsened the electronic noise performance of the system. Histograms of 100000 test pulses sent to the slow channel with equivalent charge of 1 MeV can be seen in figure 5.7. It can clearly be seen that the oscilloscope introduces noise to the system. The FWHM of the system for channel 1 with the oscilloscope probe connected was found using the normfit function of MATLAB and was found to be $2 * \sigma = 13.8 * 2 = 27.6$ ADC counts, while with the oscilloscope not connected to the analog card the FWHM was $3.2 * 2 = 6.4$ ADC counts.

The noise is usually given in terms of how many electrons are required to generate signal equivalent to the noise signal in the system. Using the calibration obtained in section 5.3.1, this is equivalent to $energy(27.6) = 459$ keV and $energy(6.4) = 56.7$ keV. This means that the electronic noise contribution to the pulse width is $6.4 = 56.7$ keV points for the slow channel, channel 1.

Noise caused by the FPGA and clock

The noise contribution of the FPGA was measured using an oscilloscope and measuring the output of channel 1 on the analog card. First, the FPGA was powered off and a fast Fourier transform of the noise signal was recorded using an oscilloscope. The FFT was recorded using 2.5 G samples per second, a 10000 point Blackman-Harris window and the root mean square value over 200 kHz was recorded. Then, the FPGA was powered on and the FFT was recorded again using the oscilloscope with the same settings. The resulting

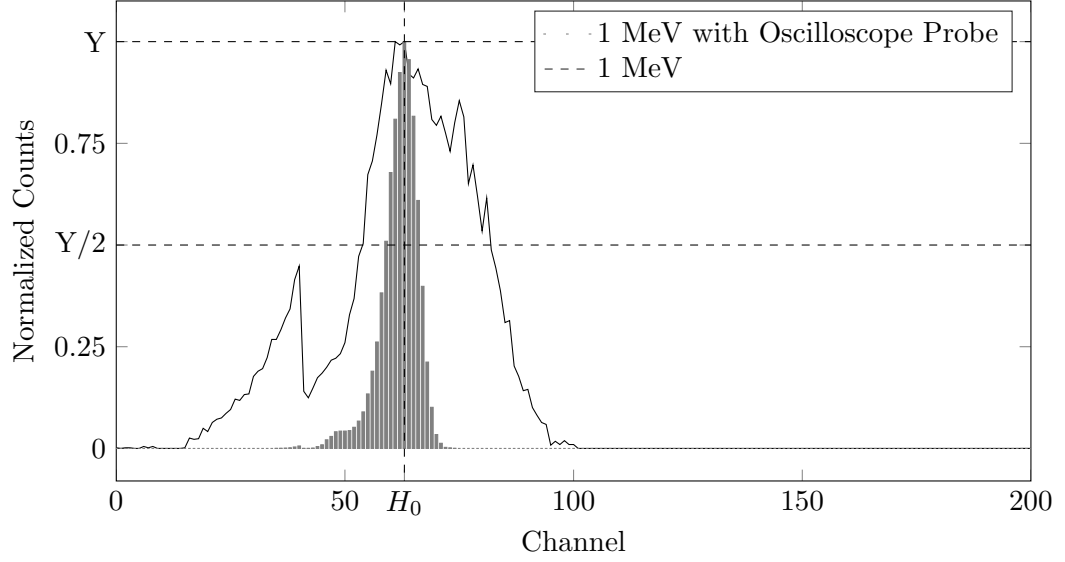


Figure 5.7: Histogram of 100000 stable test pulses sent into the slow channel, channel 1, with $C_F = 1$ pF with equivalent charge of 1 MeV. Line plot of oscilloscope probe connected to the output of channel 1. Also marked constants for energy resolution calculations used in section 6.5

FFTs can be seen in figure 5.8.

Since the sampling frequency here was much higher than the sampling frequency of the ADC, the clock feedthrough is very clearly visible at 125 MHz in figure 5.8. Aliasing is the phenomenon where a reconstructed signal appears at a lower frequency than the original. [37] Due to aliasing, the clock frequency fold back to the noise at the DC level, when sampling with the ADC. There is also noise at around 90 MHz, this seems to be interference from radio signals as it is present even when the whole circuit is powered off. This noise folds back on the FFT sampled with the ADC as well and can be seen on around 25 MHz.

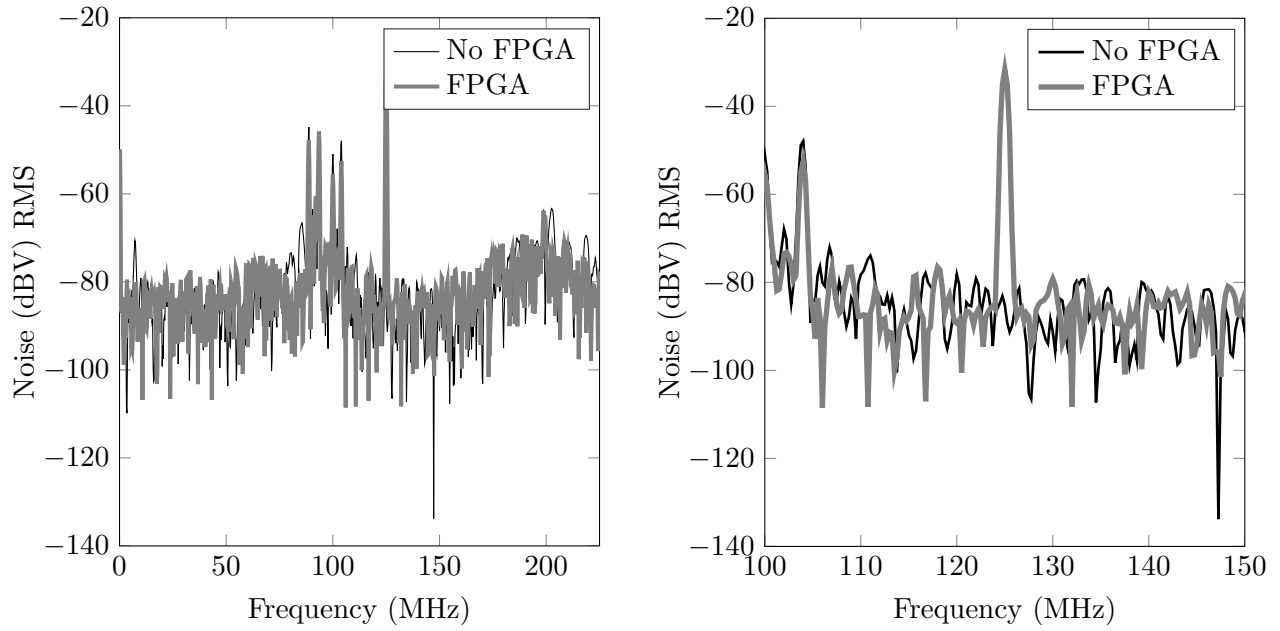


Figure 5.8: FFT of the noise signal on Channel 1 of the analog card with the the FPGA powered on and powered off. Plot on right zoomed in on 125 MHz

5.4 Radiation Spectroscopy with Radioactive Source

5.4.1 Test Setup

When choosing a radiation source the following properties of the source are important [6]:

- Category or physical form
- Radiation type
- Energy and spectral purity
- Intensity
- Half-life
- Availability, classification and cost

The two radiation sources used to characterize the system were ^{252}Cf and ^{241}Am . The properties of those two sources are summarized in table 5.4. Data about Americium 241 from [2], spontaneous fission branching from [38], data about Californium 252 branching from [39], [3] for alphas and [40] for fission fragments. Branching percentage is the probability of that particular decay occurring out of all possible decays for that particular isotope.

As can be seen in figure 5.10 and 5.11, both the ^{252}Cf and ^{241}Am sources are not directly on top of the detector and there is some air the particles have to travel through to reach it. The distance of the radioactive source to the detector is estimated to about 5mm. According to [41], alpha particles from an ^{241}Am source lose about 0.5 MeV in about 5 mm of air.

In addition to this, the surface of the silicon has a dead layer in which alpha particles lose some of their energy, which causes a broadening of the radiation peak in an energy spectrum [2]. In addition to this, the detector has a layer of about 1 μm aluminium on top of it, in which particles lose some additional energy. However as this loss is not exactly known, it is left out of the estimated energy loss estimation. The estimated energy that reaches the detector is very roughly estimated to be 0.5 MeV less than at the source and can be seen in table 5.4.

The setup of the californium source on the detector can be seen in figure 5.10 and for the americium source in figure 5.10. The schematic for the setup of the complete system can be seen in figure 5.9.

For the Americium source, the radioactive material is deposited on a stainless steel disc, with a diameter of 25mm, the active area has a diameter of 7 mm [42]. The californium source is an aluminium container with californium electroplated in a cavity. The radioactive source is placed on top of an aluminium plate with an opening with a diameter of 5 mm. The purpose of the aluminium plate is to act as a collimator so that the radiation would

Property	^{252}Cf source	^{241}Am source
Half-Life of Isotope	2.645 years	433 years
Alpha Particle Kinetic Energy (Branching)	6.118 MeV (81.6 %)	5.48574 ± 0.00012 MeV (85.2 %)
	6.076 MeV (15.2 %)	5.44298 ± 0.00013 MeV (12.8 %)
Spontaneous Fission Branching Percentage	3.6%	3.6×10^{-10} %
Kinetic Energy Fission Fragments	$80.01 \text{ MeV} \pm 0.8$	
	$105.71 \text{ MeV} \pm 1.06$	
Physical Form	25 mm aluminium holder	25 mm stainless steel holder
Source Line Width	not known	< 20 keV
Source Activity	3.7 kBq	5 kBq
Estimated Main Alpha Energy at Detector	5.61 MeV	4.98 MeV

Table 5.4: Properties of the two radiation sources used for system characterization

hit the detector and not the edge of the detector. The distance between the detector and the radiation source is approximately 5 mm.

We can use the previous information to calculate the approximate amount of radiation that will reach the detector. We know the activity of the radiation sources in units of Becquerel. We assume that the source radiates equally in all directions. We assume that half of the intensity of the source goes into the opposite direction of the detector, it gets absorbed by the metal holders. The remaining half of the intensity is collimated by the aluminium plate. The so the percentage of the radiation from the active area with radius 3.5mm reaching the detector through the opening with radius 2.5mm can be approximated to:

$$A_{\text{opening}}/A_{\text{active}} = \pi r_{\text{opening}}^2 / \pi r_{\text{active}}^2 = \pi 2.5^2 / \pi 3.5^2 = 0.5101 = 51.01\% \quad (5.1)$$

The approximate percentage of the total activity that reaches the detector is then:

$$0.5 * 0.5101 = 0.255 = 25.5\% \quad (5.2)$$

This means that the intensity at the detector is roughly 944 Bq for the ^{252}Cf source and 1.275 kBq for the ^{241}Am source. It has to be noted here that the exact date and measurement method for the given activity of the Californium source is not known. Therefore,

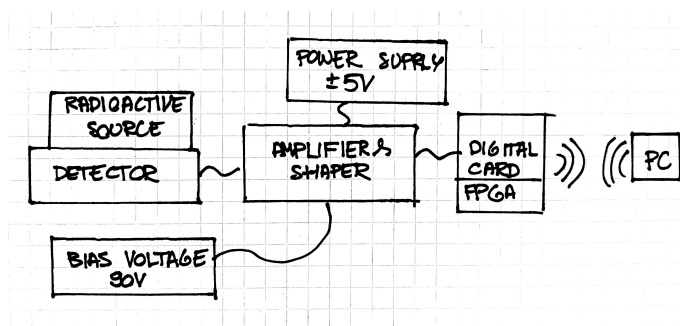


Figure 5.9: Schematic of the setup of the system described in this work for radiation testing

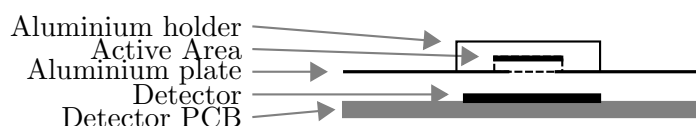


Figure 5.10: Schematic of setup of the Californium source. Not to scale

the activity level given here may be somewhat higher than the actual activity level. Approximate measurements for the activity level for Californium are detailed in section for Californium and section for Americium.

5.4.2 Pulse Pile-Up Considerations

Since radiation spectroscopy involves recording pulse height spectra, a short description of different defects in the spectra are discussed here. Because of the random nature of radiation events, there is a probability that two events interfere each other, these effects are generally called pile-up. The way to minimize pile-up is to make the width of the pulses as small as possible [2]. The first type of pile-up is called tail pile-up and means that a pulse occurs on the the tail of another pulse. An example of this can be seen in pulses measured with the system described in this work of ^{252}Cf in figure 6.3. Tails can persist for a relatively long time so that tail pile-up can be significant event at relatively low count rates. The tail pile-up can either occur while the pulse has not yet returned to

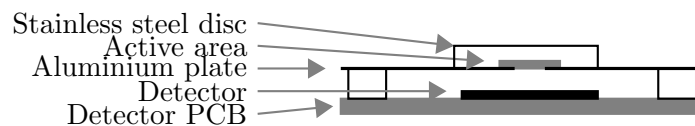


Figure 5.11: Schematic of setup of the Americium source. Not to scale

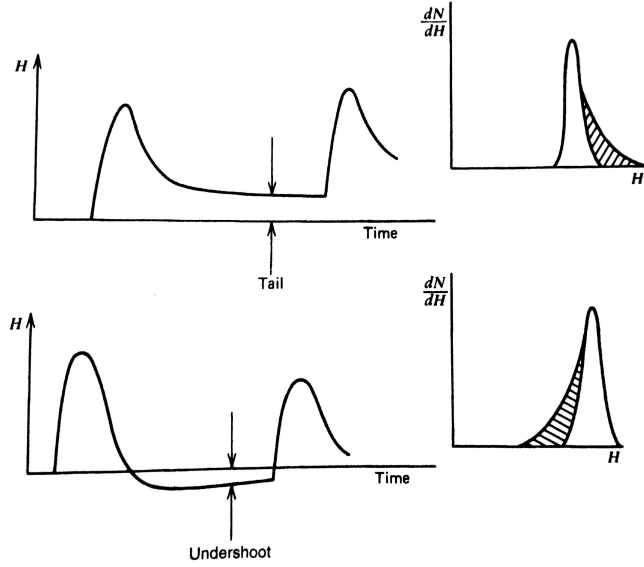


Figure 5.12: Tail pile-up effects. Top: pile-up on the tail of the preceding pulse, bottom: pile-up on the undershoot of the preceding pulse from [2]

baseline or on the undershoot of the pulse. Both pile-up types can be seen in figure 5.12. The pile-ups are removed by eliminating tails by using shaping and removing undershoot by using pole-zero correction [2]. Both of these techniques are used in this work on channel 1 and 3 on the analog card. However, we can see in figure 5.12 and 6.3 that because of the random nature of radiation events, pile-ups still occur.

Another type of pile-up, called a peak pile-up occurs when two pulses are sufficiently close together that they are treated as a same pulse by the analysis system. The resulting pulse has a height that is a combination of the two pulses [2]. A peak pile-up can be seen in actual data measured with the system from a ^{252}Cf source in figure 5.13. This type of pile-up leads to a distortion in the recorded spectrum, it also disturbs quantitative measurements based on measuring the area under the pulse. Because peak pile-up leads to the recording of one pulse instead of two, the total area under the recorded spectrum is also smaller than the total number of pulses presented to the system during its live time. The total effect of pile-ups on an energy spectrum can be seen in figure 5.14. The peak pile-ups create a continuous spectrum up to a double of the pulse heights, where the effect is most intense [2].

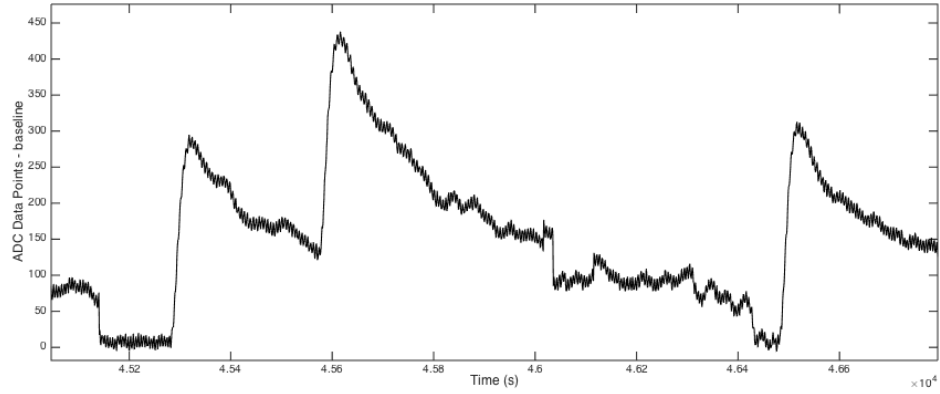


Figure 5.13: Raw pulse from ^{252}Cf source acquired with channel 1 of the system described in this work, example of peak pile-up

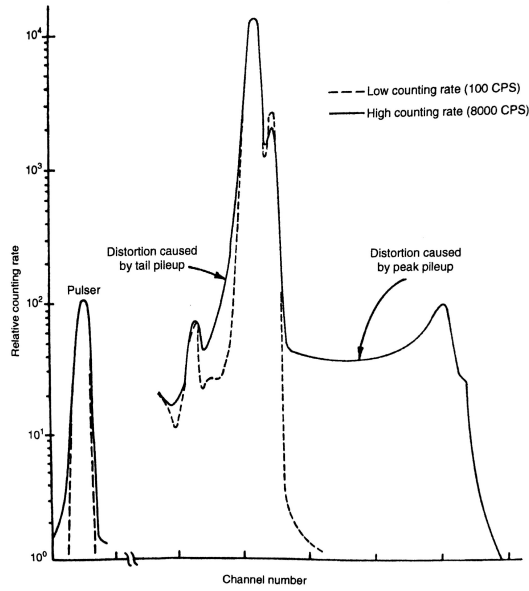


Figure 5.14: Spectral effects of peak and tail pile-up from [2]

Chapter 6

Results

6.1 Notes on Channel 2

The system has 3 channels in total, with channel 1 and 3 being identical with shaping and channel 2 being without shaping and only used for timing purposes. During testing it was concluded that it was not possible to use channel 2 with the detector because of high frequency noise. Channel 2 does not have a shaping step. Therefore, the high frequency random noise is amplified by the preamplifier and since the signal has a very low amplitude before the preamplifier, the high frequency noise had an amplitude comparable to the signal amplitude. The high frequency noise was filtered out by the test capacitor during the calibration of the card, after removing the test capacitor the noise was much more severe. This is not a problem on channel 1 and 3 because the shaping works as a band-pass filter, as described in section , and eliminates the high frequency noise from the signal. An example of the raw signal from channel 2 can be seen in figure 6.1, showing both a real signal and the high frequency noise.

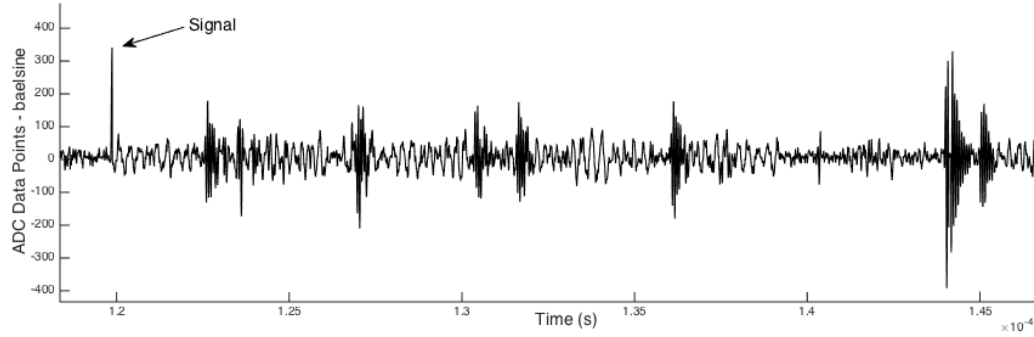


Figure 6.1: ^{252}Cf source. Pulses read out channel 2. Signal is marked with an arrow. The high frequency noise is visible, signal processing on the FPGA is turned off

6.2 Alpha and Fission Fragment Spectroscopy with ^{252}Cf source

The main alpha components of ^{252}Cf are at 6.118 MeV and 6.076 MeV. When converted to data points on the ADC using the calibration equations found in section 5.3.1, they are equivalent to 323 and 325. We know that the FWHM for channel 1 is 6.4 ADC data points at ideal conditions. This means that both of these alphas fall into one peak in the pulse height spectrum.

Example of one pulse with the equivalent charge of 6.1 MeV can be seen in figure 6.4. The equivalent charge was calculate using the calibration formula found in section 5.3.1. A sample of more pulses acquired with the system can be seen in figure 6.3.

6.2.1 Energy Spectrum

The energy spectrum is acquired by reading out the pulse heights from the FPGA. The pulse heights are plotted in MATLAB using the histogram command. A normal fit is found for the main energy lobe. The properties of the normal fit is marked on the plots.

6.2.2 Measured Intensity

The approximate predicted intensity that can reach the detector was calculated in section 5.4.1 and was found to be roughly 944 Bq for the ^{252}Cf source. To measure the actual intensity 1E6 data points were read from channel 1 with all of the signal processing modules turned off on the FPGA. The number of events was noted. The error was assumed to be uniform. To convert the amount of events to Becquerel, the following calculation was used:

$$N_{events}/time = 5/8 \mu s \pm \sqrt{5}/0.008 = 625 \text{ Bq} \pm 280 \text{ Bq} \quad (6.1)$$

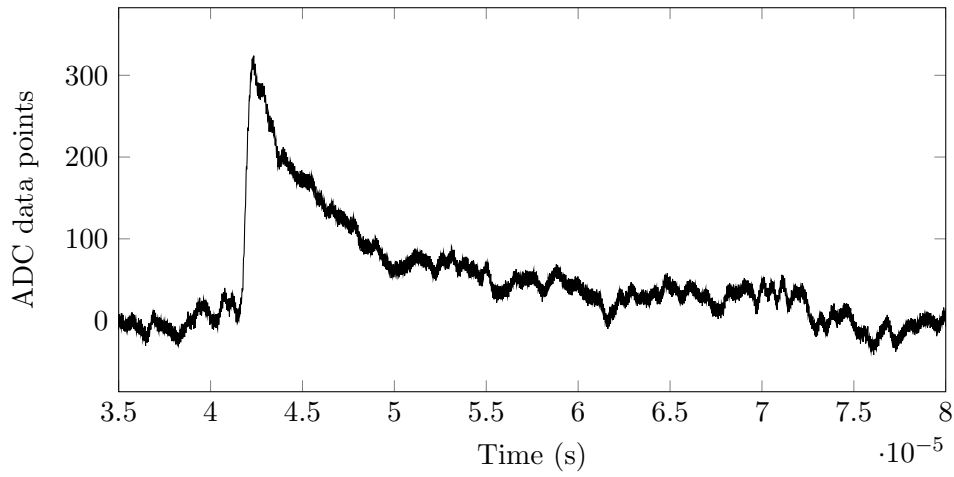


Figure 6.2: ^{252}Cf source. A pulse read out channel 1 from the FPGA with height of 324 ADC data points which corresponds to charge 6.1 MeV. Baseline trigger is set to 40

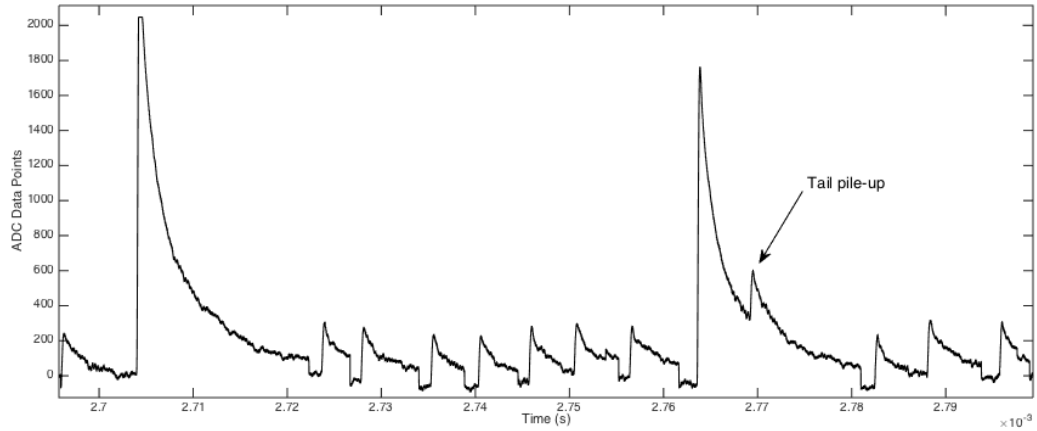


Figure 6.3: ^{252}Cf source. Pulses read out channel 1, a tail pile-up is also visible and is marked with an arrow. Zero suppression and baseline correction are applied. Baseline trigger is set to 40

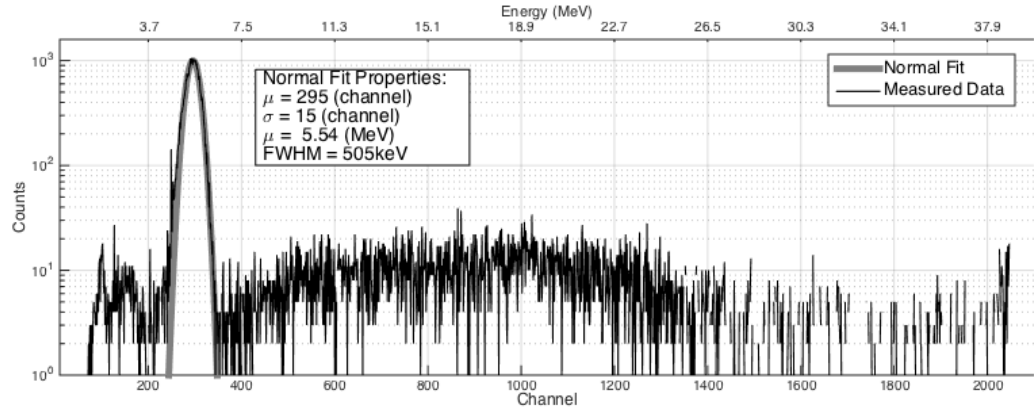


Figure 6.4: Californium 252 energy spectrum, logarithmic Y axis, acquired with channel 1, 5E4 pulse heights. Baseline trigger is set to 40

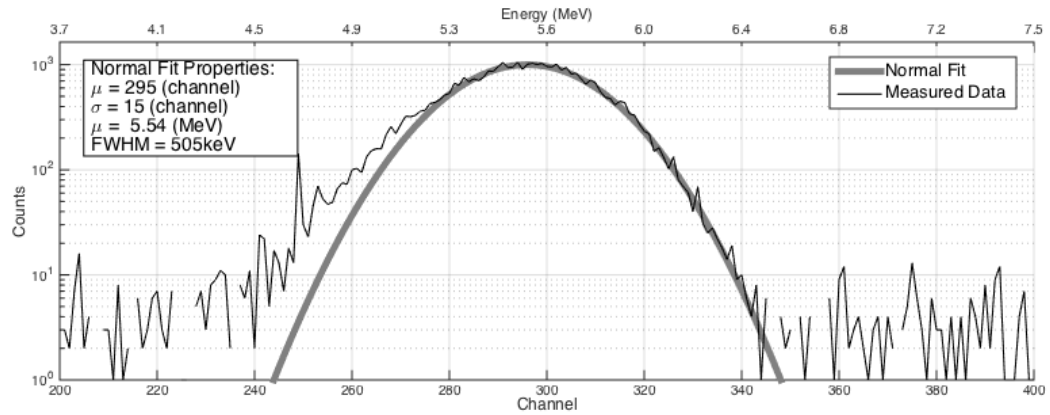


Figure 6.5: Californium 252 energy spectrum, logarithmic Y axis, acquired with channel 1, 5E4 pulse heights, zoomed in on main lobe, plotted with normal fit. Baseline trigger is set to 40

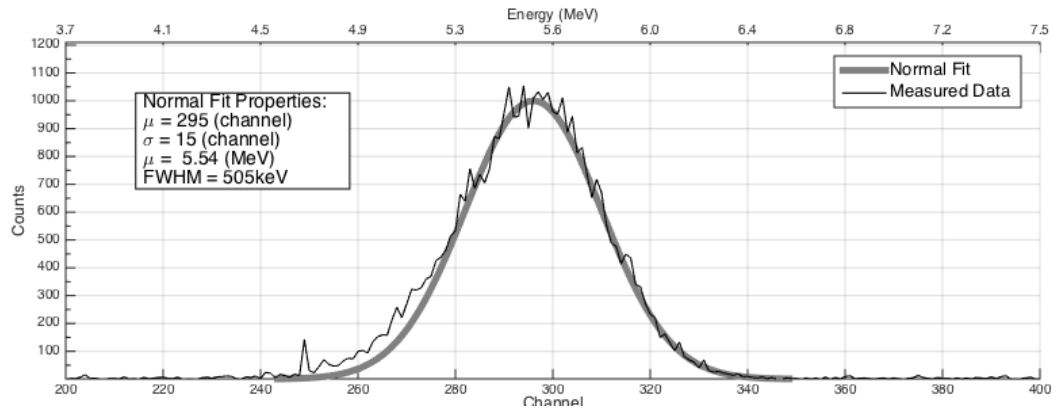


Figure 6.6: Californium 252 energy spectrum, linear Y axis, acquired with channel 1, 5E4 pulse heights, zoomed in on main lobe, plotted with normal fit. Baseline trigger is set to 40

The amount of events during the data gathered is not enough to form a result with good statistics. However, we can see that the approximate estimated is somewhat higher than the measured intensity. As discussed in the previous section, the time of the measurement of the source activity is not known exactly. Therefore, considering the relatively short half life of the isotope, the measured lower intensity is plausible.

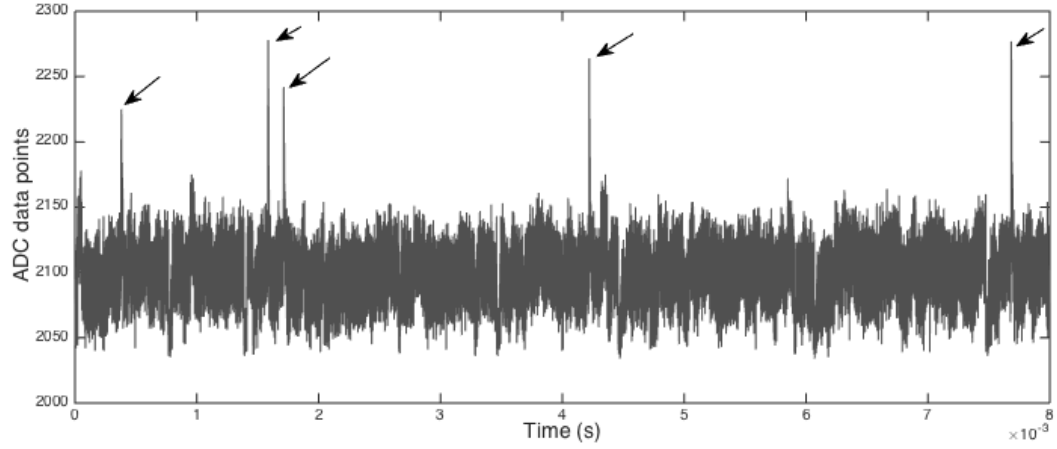


Figure 6.7: Plot of data acquired from channel 1 from ^{252}Cf source, 1E6 points, all digital signal processing turned off, events marked with arrows. Baseline trigger is set to 40

6.3 Alpha Spectroscopy with ^{241}Am source

The test with the ^{241}Am source was set up the same way as with the ^{252}Cf spectrum. Baseline level in all measurements is 40. An example of raw pulses read out of channel 1 can be seen in figure 6.8.

6.3.1 Energy Spectrum

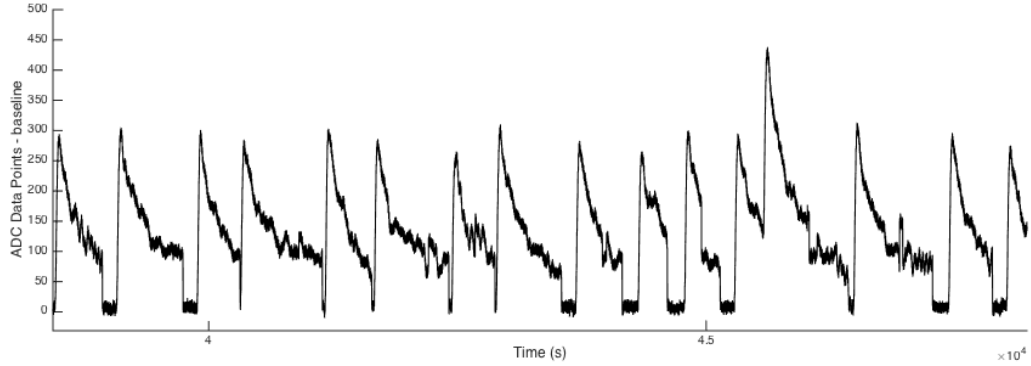


Figure 6.8: ^{241}Am source. Pulses read out channel 1. Zero suppression and baseline correction are applied. Baseline trigger is set to 40

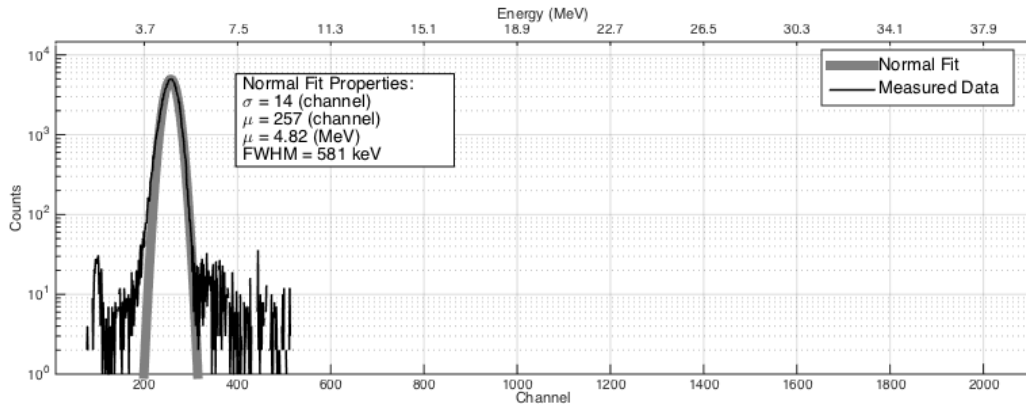


Figure 6.9: Complete Americium 241 energy spectrum, logarithmic Y axis, acquired with channel 1, 2E5 pulse heights, 5000 counts at the main lobe center

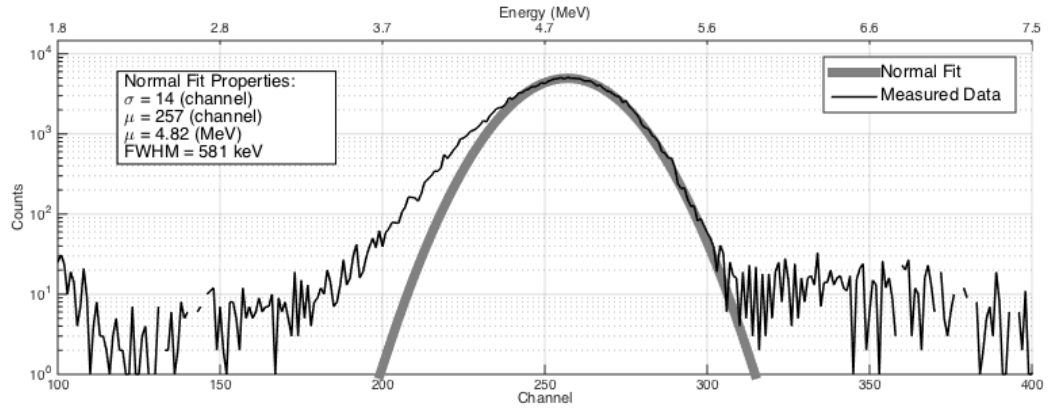


Figure 6.10: Americium 241 energy spectrum, logarithmic Y axis, acquired with channel 1, 2E5 pulse heights, 5000 counts at the main lobe center, zoomed in on the main lobe

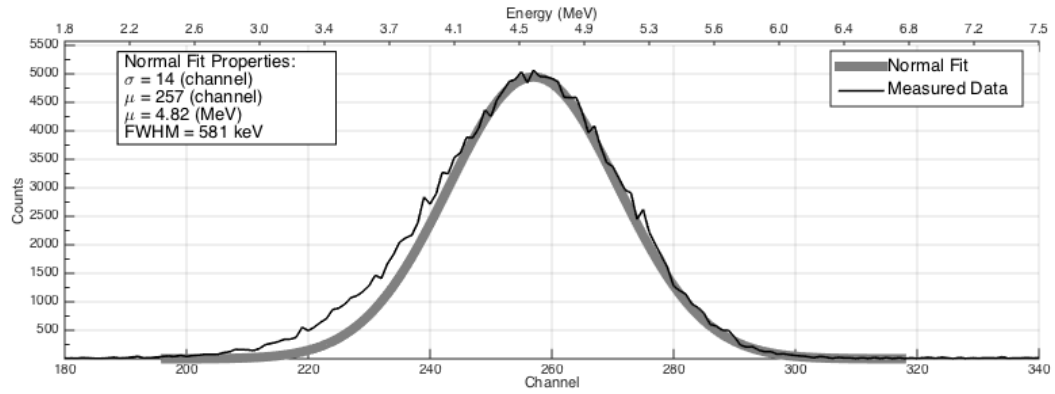


Figure 6.11: Americium 241 energy spectrum, linear Y axis, acquired with channel 1, 2E5 pulse heights, 5000 counts at the main lobe center, zoomed in on the main lobe

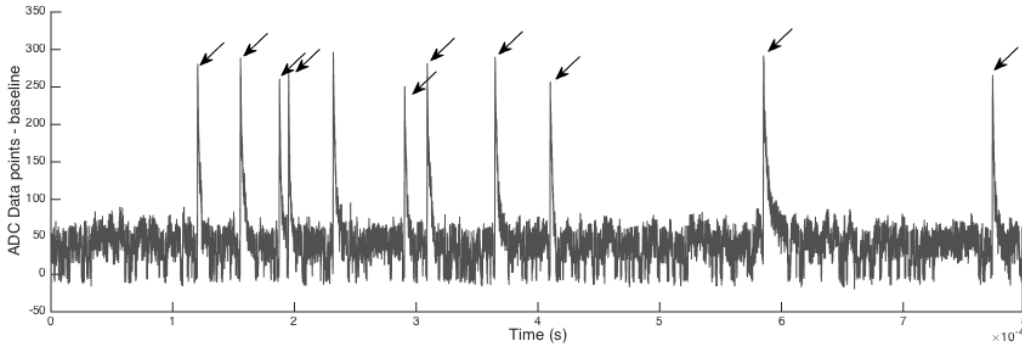


Figure 6.12: Plot of data acquired from channel 1 from ^{241}Am source, $1\text{E}5$ points, all digital signal processing turned off, events marked with arrows. Baseline trigger is set to 40

6.3.2 Measured Intensity

The data for intensity measurement was gathered by turning off all of the signal processing modules on the FPGA. The data can be seen in figure 6.12.

$$N_{events}/time = 11/798 \text{ ns} \pm \sqrt{11}/798 \text{ ns} = 1.34 \text{ kBq} \pm 416 \text{ Bq} \quad (6.2)$$

The intensity for ^{241}Am is within the limits of the estimated intensity from section 5.4.1.

6.4 Summary of Results of the Radiation Testing

This was accomplished and the results of the measurements can be seen in chapter 6. The main energy component of ^{252}Cf source was measured at 5.54 MeV, with a FWHM of 505 keV. The estimated intensity was 944 Bq, the measured intensity was $625 \text{ Bq} \pm 280 \text{ Bq}$.

The main component in the spectrum of ^{241}Am was measured at 4.82 MeV, with a FWHM of 581 keV. The estimated intensity was 1.275 kBq, the measured intensity was $1.34 \text{ kBq} \pm 416 \text{ Bq}$.

Another way to evaluate the accuracy of the system is to look at the theoretical difference of alpha energies from ^{241}Am at 5.486 MeV and ^{252}Cf at 6.118 MeV. The difference between these two energies is $6.118 \text{ MeV} - 5.486 \text{ MeV} = 632 \text{ keV}$. The difference between the two measured energies is $5.54 \text{ MeV} - 4.82 \text{ MeV} = 720 \text{ keV}$.

6.5 Measured Energy Resolution of the System

One important property of a detector in radiation spectroscopy can be found by noting its response to a monoenergetic radiation. If the width of the response peak is wide, it

indicates a large fluctuation was recorder from pulse to pulse even though the same energy was deposited to the detector for each event. The formal definition of the energy resolution R of the detector is:

$$R = \frac{FWHM}{H_0} \quad (6.3)$$

where H_0 is the location of the peak centroid. The energy resolution R is therefore a dimensionless fraction expressed in percentages. The smaller the percentage, the better the detector can distinguish between two radiations which energies are near each other. [2]

The ideal resolution of the system was calculated for bot Americium and Californium. For Americium the measured resolution was:

$$\begin{aligned} Y &= 5000 \\ Y/2 &= 2500 \\ H_0 &= 257 \\ FWHM(H_0) &= 34 \\ R &= \frac{34}{257} = 0.1323 = 13.23\% \end{aligned} \quad (6.4)$$

For Californium the measured resolution was:

$$\begin{aligned} Y &= 1000 \\ Y/2 &= 500 \\ H_0 &= 295 \\ FWHM(H_0) &= 32 \\ R &= \frac{32}{295} = 0.1085 = 10.85\% \end{aligned} \quad (6.5)$$

Where Y is the number of counts at peak with center at H_0 , all of the constants used in this equation are marked on a pulse height spectrum in figure 5.7. The rule of thumb is that one should be able to resolve energies that are separated by more than one value of the FWHM. [2] For channel 1 and 3 this means, using the calibration obtained in section 5.3.1, that the the system can distinguish two energies that are at least $x(2048) * 10.17\% = 39.33 \text{ MeV} * 0.1323 = 5.2 \text{ MeV}$.

Chapter 7

Discussion and Conclusion

7.1 Discussion of the Design of a Portable System for Radiation Detection

The two main goals of the thesis were to design analog front-end electronics to interface a silicon PIN detector to a digital signal processing back-end and to make the complete system easy to use and set up and portable.

The first main goal was completed and the design of the analog electronics were tested both theoretically in LTSpice and in practice by assembling several test cards to test both the complete amplifier and specifically the preamplifier. The system was characterized by using both test pulses generated by a signal generator and by using radioactive sources. The noise characteristics of the system were measured and the electronic noise contribution to the pulse width was found to be 56.7 keV or 6.4 points of the ADC data points. The linearity of the system was measured, the calibration equations to convert ADC data points to energy were calculated and the integral nonlinearity for channels 1 and 3 was found to be 1.27% and 0.1% for channel 2.

The goal of making the system easy to use and set up was fully met in the opinion of the author. To use the system, one needs two laboratory power supplies and a personal computer with wireless connectivity. Laboratory power supplies are standard equipment in any cyclotron and radiation measuring facility. All of the settings of the system are easily changed from the Java program written for the system and all data is easily acquirable from within the program.

7.2 Discussion of the Characterization of the System with ^{241}Am and ^{252}Cf

The third main goal of the thesis was to characterize the system by using radioactive sources Americium 241 (^{241}Am) and Californium 252 (^{252}Cf). This was accomplished and the results of the measurements can be seen in chapter 6. The main energy component of ^{252}Cf source was measured at 5.54 MeV, with a FWHM of 505 keV. The measured energy correspond well to the estimation from section 5.4.1. The large FWHM value is caused by in part the electronic noise of the system and more importantly by the pulse pile-up effects discussed in section 5.4.2. One can also see that although the main alpha component is most prominent in the energy spectrum, the fission products produced by the spontaneous fission are also visible in the energy spectrum. Energies up to the maximum detectable value of the system were measured. This is proof that the system is capable of measuring fission fragments. However, the main fission fragments of ^{252}Cf are currently out of range of the system described in this thesis, as they have energies 80.01 MeV and 105.71 MeV [2]. However, by modifying the sensitivity of the preamplifier and the gain of the amplifier, these energies can be seen. Unfortunately, due to time constraints these measurements were not performed.

The main component in the spectrum of ^{241}Am was measured at 4.82 MeV, with a FWHM of 581 keV. Also here, the measured energy correspond well to the estimation. The large FWHM value is caused by in part the electronic noise of the system, the pulse pile-up effects discussed in section 5.4.2 and the fact that the main lobe of the spectrum includes both the 5.48 MeV and the 5.44 MeV energies. The spectrum widening more on the lower channels for the ^{241}Am corresponds well to the spectrum measured with a high resolution system, that can be seen in figure 2.3. The widening of the spectrum on the lower channels is more visible on the logarithmic plot of the spectrum in figure 6.10. The effect of the peak pile-up described in section 5.4.2, counts between the main measured energy and up to twice the measured energy can be observed in the spectrum.

The resolution of the system was measured to be 10.85% for ^{252}Cf and 13.23% for ^{241}Am .

7.3 Discussion of Using Different Types of Detectors and Detecting Various Types of Radiation

Currently, the system has been successfully tested with a silicon PIN detector. However, the output of many of the semiconductor detectors is very similar [2], a current pulse. Therefore, the system can successfully be interfaced with other types of semiconductor detectors. For example Germanium or lithium drifted silicon detectors described in [2]. The exact performance of the system with these detectors needs to be tested. However, using these detectors should not require any modifications to the system.

The system can easily be interfaced to a scintillation detector as well. The electronics needed to interface a scintillation detector to the system described in this thesis, is a photomultiplier tube [2], which can then directly be connected to the preamplifier. The photomultiplier converts the light photons produced by a scintillation detector to electrons and multiplies them, so that the output is a number of electrons large enough to be converted to a voltage pulse by a preamplifier [2]. The photomultiplier outputs pulses much in the same way a semiconductor detector does and the electronics can therefore be used interchangeably.

Another type of detector that can be interfaced with the system without any modifications needed is the thin film breakdown counter. The counter would need an external biasing network and can then be connected directly to the window comparator inputs of the digital card, this is described in more detail in section 3.12. The pulses generated by the thin film breakdown counter are compared to trigger thresholds by the window comparators on the digital card and the pulses output by the comparators are counted by the FPGA. The system is therefore directly compatible with this type of detector.

The system, together with a silicon PIN detector, was successfully used to detect alpha particles from ^{252}Cf and ^{241}Am and fission products from ^{252}Cf . Since the system can be used together with a TFBC, fission fragments can be detected using a TFBC with a natural uranium target and a proton beam. This has been tested in [43] with a natural tungsten target and a proton beam. This enables the measurement of the flux of the proton beam at the cyclotron facility at the University of Oslo. As the reaction mechanics, induced fission, is the same for both tungsten and uranium, the general concept is therefore shown to work. Although this type of measurement has not yet been performed with the system described in this thesis, it is an interesting continuation for the work done.

7.4 Suggestions for Future Improvements of the System

This relatively large number of the electronic noise in the system is caused by the low amplification in the system. As the system was to be used to also measure ^{252}Cf fission fragments, the amplification was kept low. As a future improvement, the noise performance of the system can be greatly improved by increasing the amplification of the amplifier on the analog card. This would also improve the resolution of the system, which was measured in section 6.5. As the resolution calculation is dependent on the channel number, raising the amplification would move the pulse higher up in the channel without increasing the width of the pulse height spectrum. Ideally, the sensitivity of the system could also be changed by varying the feedback capacitor on the preamplifier. This would allow the system to measure higher energies.

A strategy to minimize the noise from the detector is to either cool the detector or perform the tests in vacuum [2]. To evaluate the true system performance, these two test scenarios could be explored in the future.

The system could also be evaluated more precisely if measured together with a well calibrated commercial system, this would remove many of the uncertainties around the radiation sources used. Specifically, the energy of the radiation reaching the detector and the activity of the sources, which could only be roughly estimated now.

The system amplifier gain and preamplifier sensitivity can be modified to customize the system specifically for the type of radiation one wishes to measure. As described earlier in this chapter, the modifications to the gain of the system could also improve the overall performance.

7.5 Conclusion

A working radiation detection system was developed and tested. The results show that the system works and can successfully be used in characterizing alpha sources. The main goals of the system have therefore been accomplished:

- Front-end electronics were designed and tested with a silicon PIN detector
- The designed system is easy to set up and is portable and should be intuitive to use
- The system was characterized using alpha sources Americium 241 (^{241}Am) and Californium 252 (^{252}Cf)
- The possibility of using different types of detectors and detecting various types of radiation with the system described in this thesis was discussed

Bibliography

- [1] M. Z. M.J. Berger, J.S. Coursey and J. Chang, “Estar, pstar, and astar: Computer programs for calculating stopping-power and range tables for electrons, protons, and helium ions (version 1.2.3),” 2005.
<http://physics.nist.gov/Star> (01.04.2015).
- [2] G. F. Knoll, *Radiation Detection and Measurement*. Ann Arbor, Michigan: Hamilton Printing Company, 2010.
- [3] H. Gulkanyan and A. Margaryan, “Alpha-spectroscopy of cf-252 decays: A new approach to searching for the octoneutron,” *arXiv preprint arXiv:1409.1772*, 2014.
- [4] T. Instruments, *INA3221 - Triple-Channel, High-Side Measurement, Shunt and Bus Voltage Monitor with I2C Interface*. Texas Instruments.
<http://www.ti.com/lit/ds/symlink/ina3221.pdf> (01.04.2015).
- [5] E. J. Oltedal, “Fpga based readout of a silicon pin detector,” 2015. Not yet published.
- [6] G. A. Johansen and P. Jackson, *Radioisotope Gauges for Industrial Process Measurements*. West Sussex, England: John Wiley & Sons Ltd, 2004.
- [7] R. M. Barnett, G. Conforto, K. Hayes, N. Törnqvist, M. Roos, R. Schindler, S. Eidelman, L. Montanet, K. A. Olive, C. Grab, *et al.*, “Review of particle physics. particle data group,” *Phys. Rev.*, vol. 54, pp. 1–720, 1996.
- [8] P. Rinard, “Neutron interactions with matter,” *Passive Nondestructive Assay of Nuclear Materials*, pp. 357–377, 1991.
- [9] A. Belyaev, “Lecture phys3002 - 10 nuclear fission,” 2014.
<http://www.personal.soton.ac.uk/ab1u06/teaching/phys3002/notes.html> (06.04.2015).
- [10] A. Iljinov and M. Mebel, “Induced nuclear fission accompanied by pion emission,” *Physics of Atomic Nuclei*, vol. 64, no. 8, pp. 1386–1391, 2001.

- [11] R. C. Baumann, "Radiation-induced soft errors in advanced semiconductor technologies," *Device and Materials Reliability, IEEE Transactions on*, vol. 5, no. 3, pp. 305–316, 2005.
- [12] A. Corporation, *Cyclone V Device Handbook*. Altera Corporation, 2015.
https://www.altera.com/en_US/pdfs/literature/hb/cyclone-v/cyclone5_handbook.pdf (06.04.2015).
- [13] J. K. Bekkeng, "Radiation effects on space electronics." University Lecture, 2011.
<http://www.uio.no/studier/emner/matnat/fys/FYS4220/h11/undervisningsmateriale/forelesninger-vhdl/Radiation%20effects%20on%20space%20electronics.pdf> (06.04.2008).
- [14] H. Hughes and J. Benedetto, "Radiation effects and hardening of mos technology: devices and circuits," *Nuclear Science, IEEE Transactions on*, vol. 50, no. 3, pp. 500–521, 2003.
- [15] L. Tommasino, N. Tommasino, P. Klein, and Solomon, "Thin-film breakdown counter of fission fragments," *Journal of applied physics*, vol. 46, no. 4, p. 1484, 1975.
- [16] G. Van der Plas, G. Gielen, and W. M. C. Sansen, *A Computer-aided Design and Synthesis Environment for Analog Integrated Circuits*. Analog Circuits and Signal Processing, Boston: Kluwer Academic Publishers, 2002.
- [17] L. Technology, *LTC1393 - Differential 4-Channel Analog Multiplexer with SMBus Interface*. Linear Technology.
<http://cds.linear.com/docs/en/datasheet/138093f.pdf> (01.04.2015).
- [18] K. M. Tony Chan Carusone, David Johns, *Analog Integrated Circuit Design*. Singapore: John Wiley and Sons Inc, 2013.
- [19] S. Tavernier, *Experimental Techniques in Nuclear and Particle Physics*. Springer-Verlag Berlin Heidelberg, 2010.
- [20] T. Instruments, *OPA 695 - Low-Noise, High-Precision, JFET-Input OPERATIONAL AMPLIFIER*. Texas Instruments.
<http://www.ti.com/lit/ds/symlink/opa827.pdf> (01.04.2015).
- [21] A. Devices, *ADA4817 - Low Noise, 1 GHz FastFET Op Amp*. Analog Devices.
http://www.analog.com/media/en/technical-documentation/data-sheets/ADA4817-1_4817-2.pdf (01.04.2015).
- [22] T. Instruments, *OPA695 - Ultra-Wideband, Current-Feedback Operational Amplifier With Disable*. Texas Instruments.
<http://www.ti.com/lit/ds/symlink/opa695.pdf> (01.04.2015).

- [23] L. Technology, *LT1122 - Fast Settling, JFET Input Operational Amplifier*. Linear Technology.
<http://cds.linear.com/docs/en/datasheet/1122fb.pdf> (01.04.2015).
- [24] A. Giachero, C. Gotti, M. Maino, and G. Pessina, "Current feedback operational amplifiers as fast charge sensitive preamplifiers for photomultiplier read out," *Journal of Instrumentation*, vol. 6, no. 05, p. P05004, 2011.
- [25] L. Technology, *LTC6409 - 10GHz GBW Differential Amplifier ADC Driver*. Linear Technology.
<http://cds.linear.com/docs/en/datasheet/6409fa.pdf> (01.04.2015).
- [26] L. Technology, *LTC2242-10 - 10-Bit 250Msps ADC Rev. D*, 2011.
<http://cds.linear.com/docs/en/datasheet/224210fd.pdf> (01.04.2015).
- [27] T. Instruments, "Lvds product selection: The benefits of lvds in an ever-increasing portfolio of products," 2011.
<http://www.ti.com/lit/wp/snoa840/snoa840.pdf> (01.04.2015).
- [28] L. Technology, *LTC2283 - Dual 12-Bit, 125Msps Low Power 3V ADC*. Linear Technology.
<http://cds.linear.com/docs/en/datasheet/2283fb.pdf> (01.04.2015).
- [29] IDT, *IDT5V49EE501 - EEPROM Programmable Clock Generator*, 2012.
<https://www.idt.com/document/dst/5v49ee501-datasheet> (01.04.2015).
- [30] M. Integrated, *MAX9108 - 25ns, Quad, Low-Power, TTL Comparators*. Maxim Integrated.
<http://datasheets.maximintegrated.com/en/ds/MAX9107-MAX9109.pdf> (01.04.2015).
- [31] L. Technology, "High speed adc products," 2007.
http://cds.linear.com/docs/en/solutions-manual/High_Speed_ADC_Products.pdf (01.04.2015).
- [32] L. Halbo, *Electronic Components, Packaging and Production*. Falch AS, 1993.
- [33] T. Instruments, "The bypass capacitor in high-speed environments," 1996.
<http://www.ti.com/lit/an/scba007a/scba007a.pdf> (16.04.2015).
- [34] Arrow, "Socket user manual (rev. d hardware)."
<http://www.terasic.com.tw/cgi-bin/page/archive.pl?Language=English&CategoryNo=167&No=816&PartNo=4>(01.05.2015), 2014.
- [35] U. fkl, "Concurrent tcp server using select api in linux c."
<http://forum.codecall.net/topic/64205-concurrent-tcp-server-using-select-api-in-linux-c/>(01.05.2015), 2011.

- [36] MathWorks, “Linear regression.”
http://se.mathworks.com/help/matlab/data_analysis/linear-regression.html(01.05.2015).
- [37] A. Ambardar, *Digital Signal Processing-A Modern Introduction*. Thomson-Engineering, 2006.
- [38] N. K. K. . P. Chechev, “Lne – lnhb/cea –table de radionucleides.”
www.nucleide.org/DDEP_WG/Nuclides/Am-241_tables.pdf (01.05.2015).
- [39] M. Schmorak, “Www table of radioactive isotopes - cf252.”
<http://ie.lbl.gov/toi/nuclide.asp?iZA=980252&sortG=D&sortA=E>(01.05.2015), 1988.
Update: 1-Jan-1997, Y. Akovali.
- [40] S. L. Whetstone Jr, “Coincident time-of-flight measurements of the velocities of cf 252 fission fragments,” *Physical Review*, vol. 131, no. 3, p. 1232, 1963.
- [41] K. Yu, C. Yip, D. Nikezic, J. Ho, and V. Koo, “Comparison among alpha-particle energy losses in air obtained from data of srim, icru and experiments,” *Applied radiation and isotopes*, vol. 59, no. 5, pp. 363–366, 2003.
- [42] Eckert and Ziegler, “Alpha spectrometry sources.”
www.nucleide.org/DDEP_WG/Nuclides/Am-241_tables.pdf (01.05.2015).
- [43] V. Eismont, N. Filatov, A. Smirnov, S. Soloviev, J. Blomgren, H. Conde, A. Prokofiev, and S. Mashnik, “Measurements of nucleon-induced fission cross-sections of separated tungsten isotopes and natural tungsten in the 50-200 mev energy region,” *arXiv preprint nucl-ex/0507013*, 2005.

Appendices

Appendix A

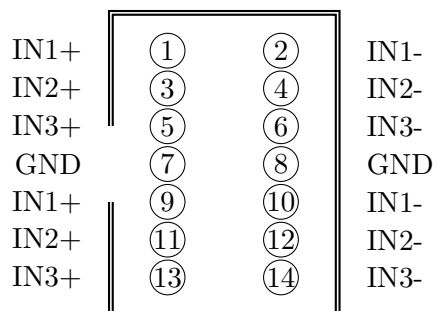


Figure A.1: Connector for current measuring on the digital card.

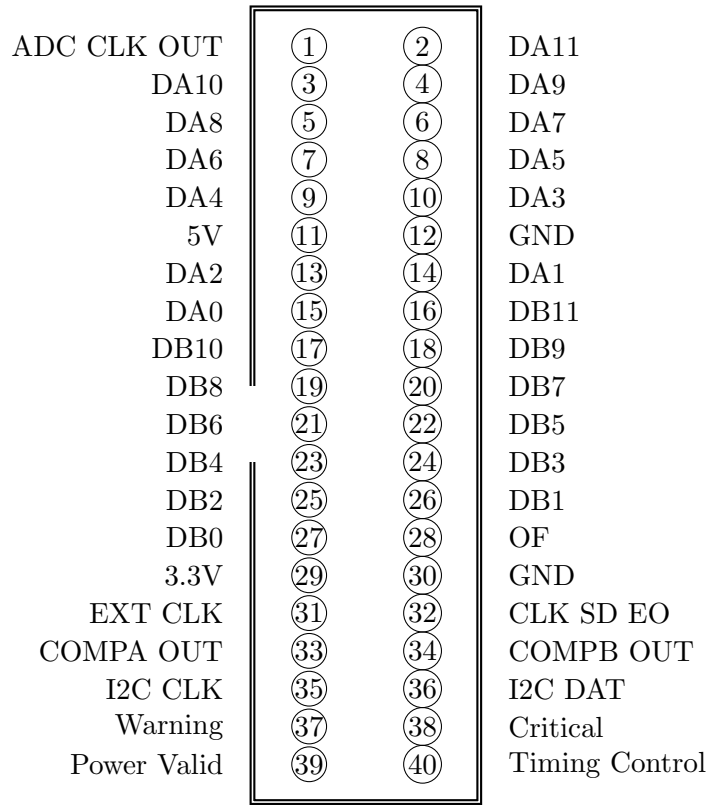
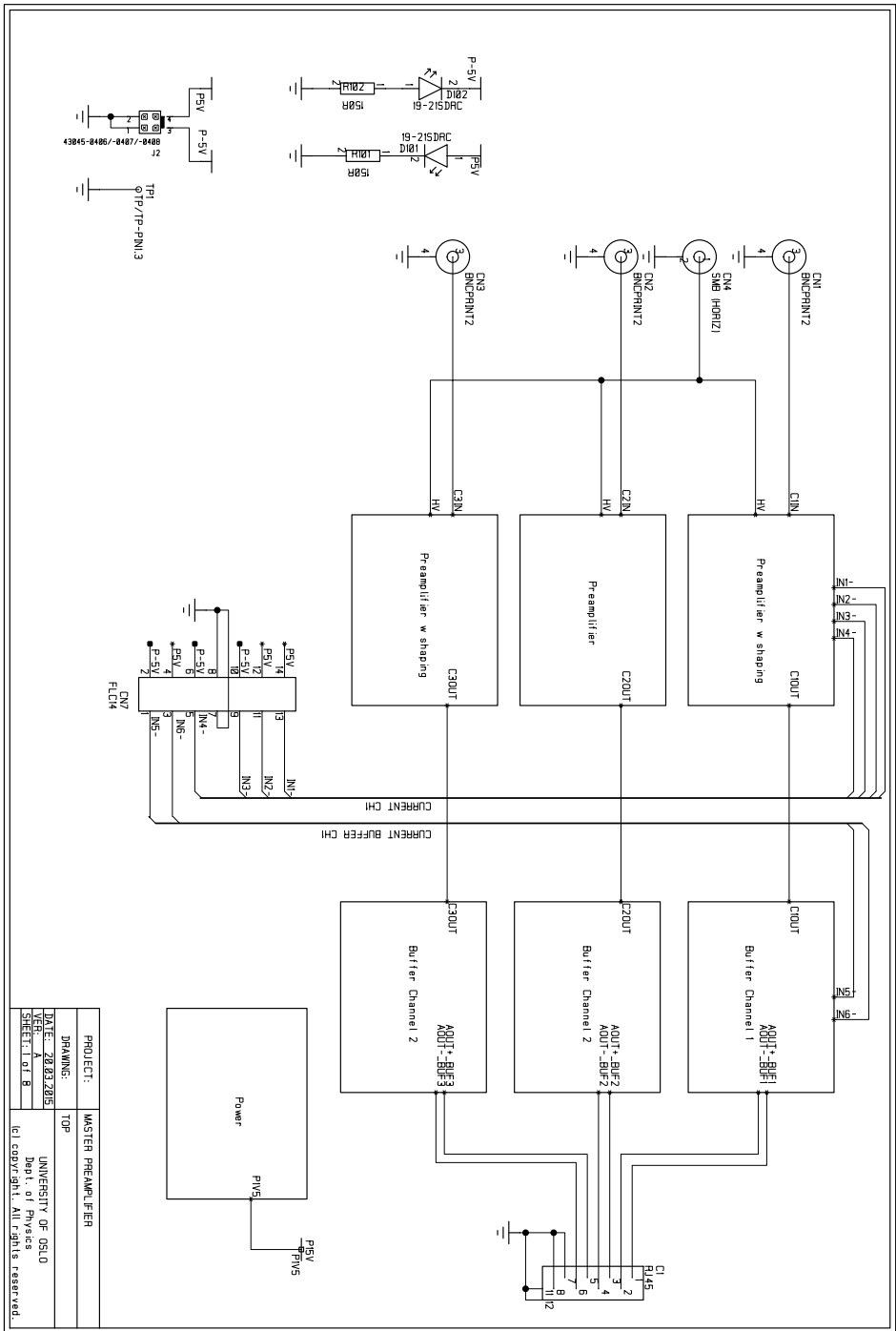
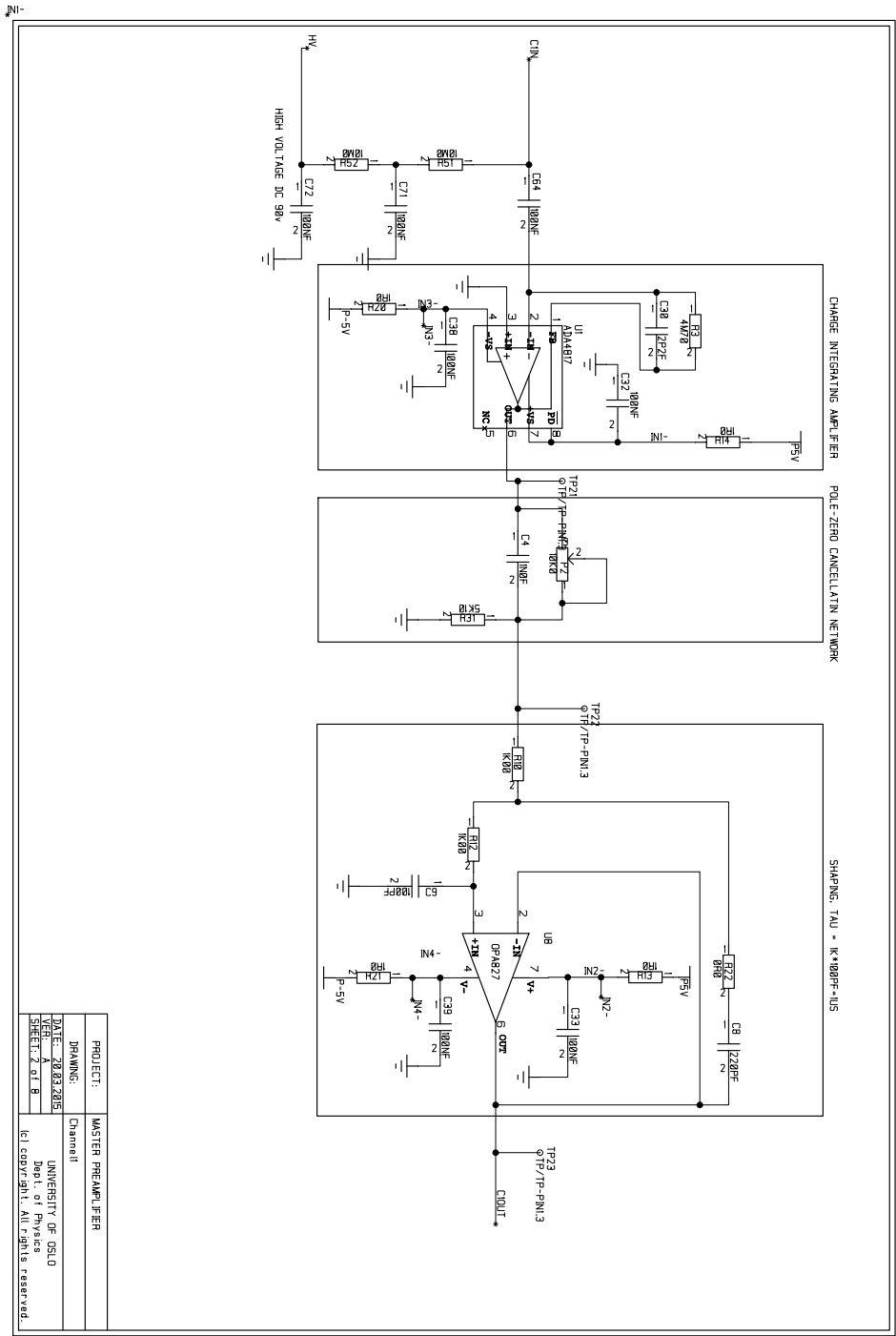
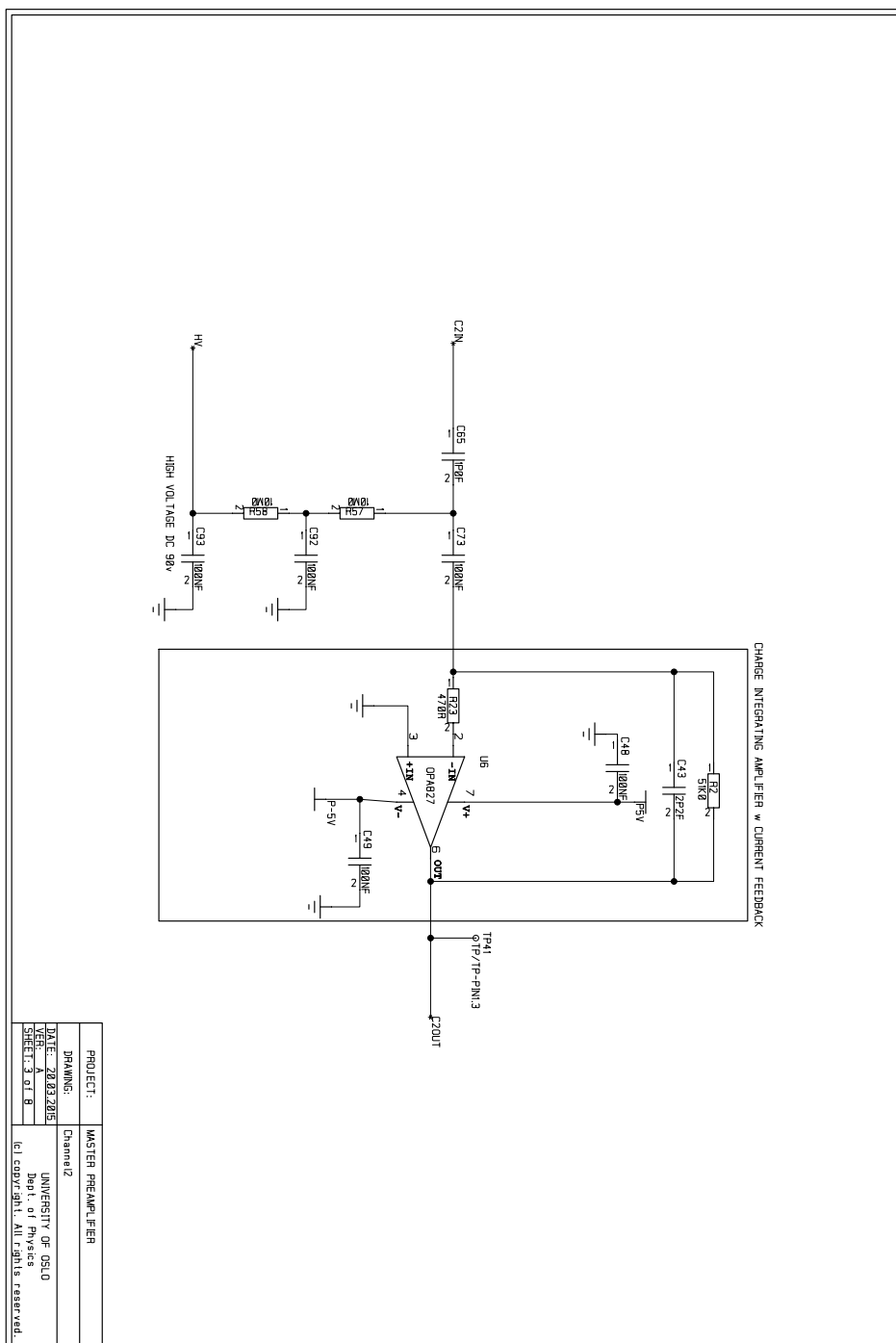


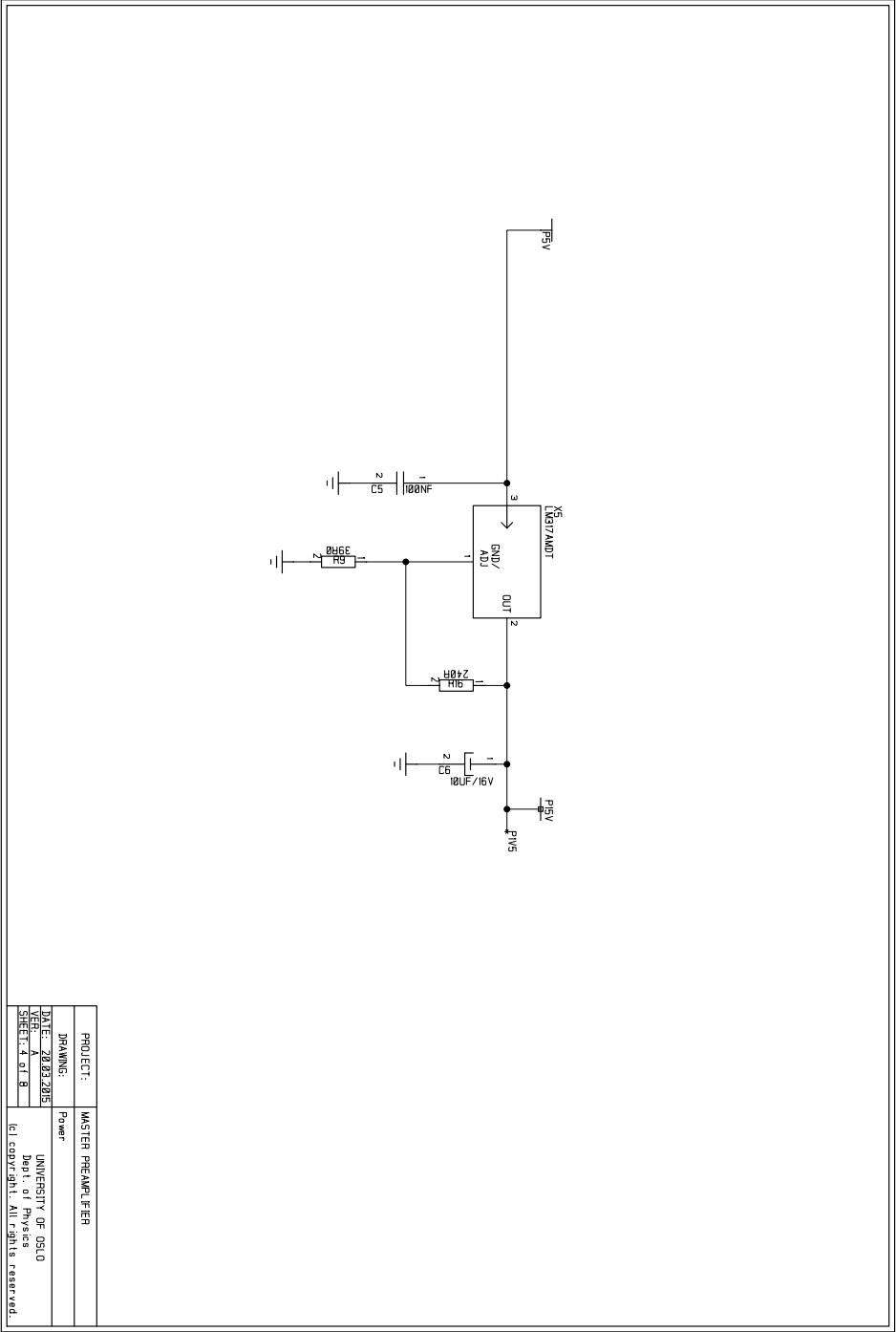
Figure A.2: Connector for the FPGA on the digital card.

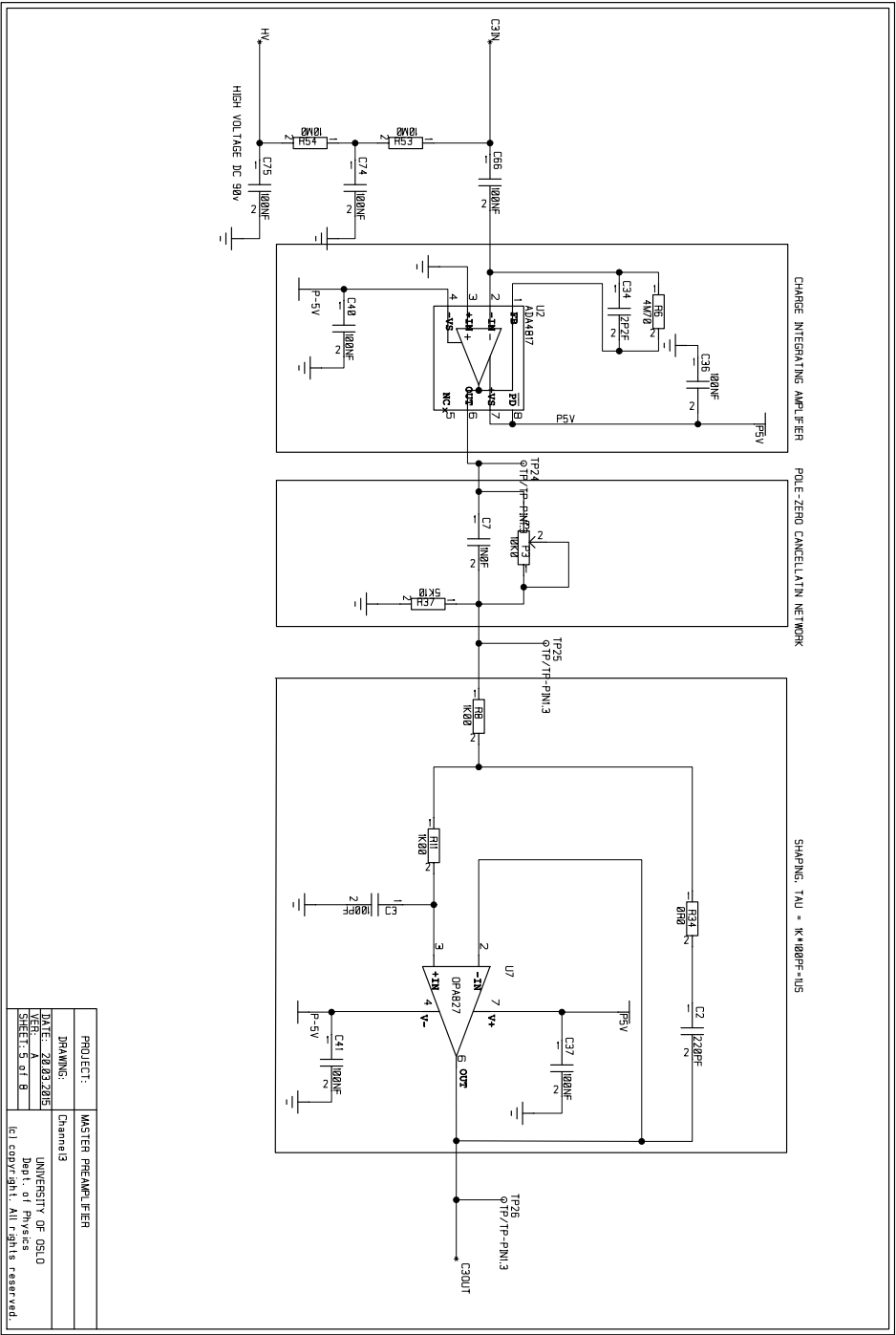
The complete schematics of the final analog PCB design

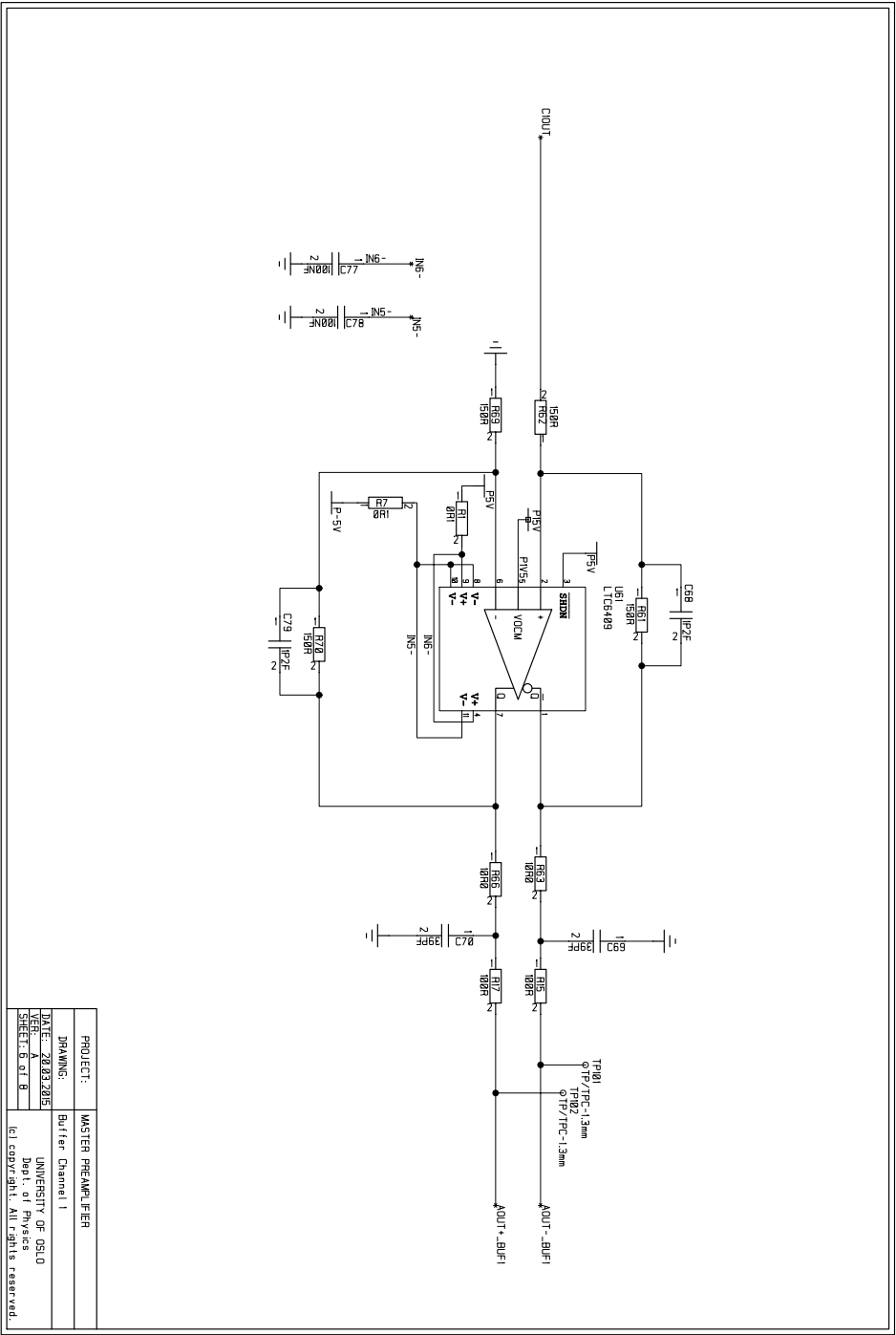


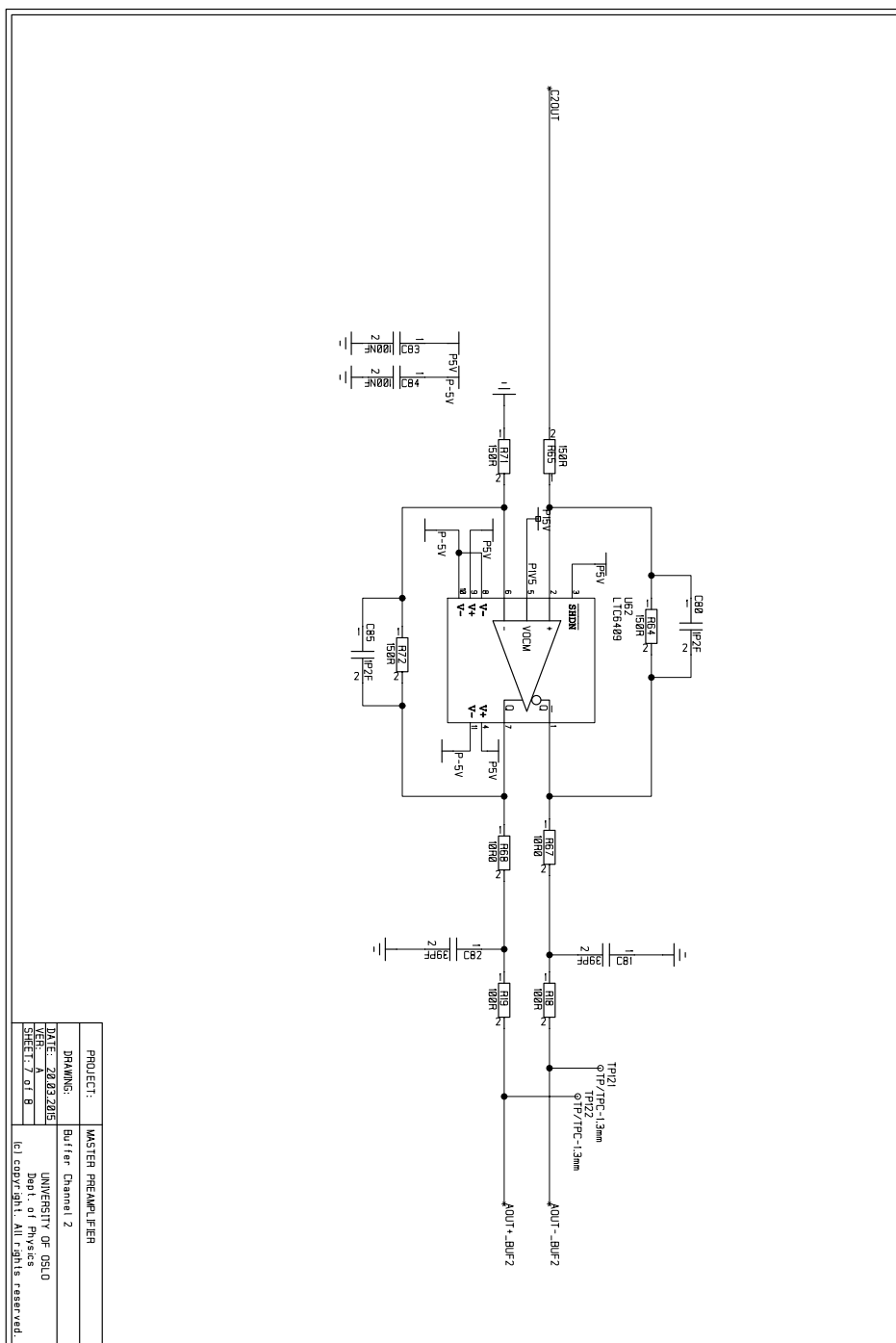


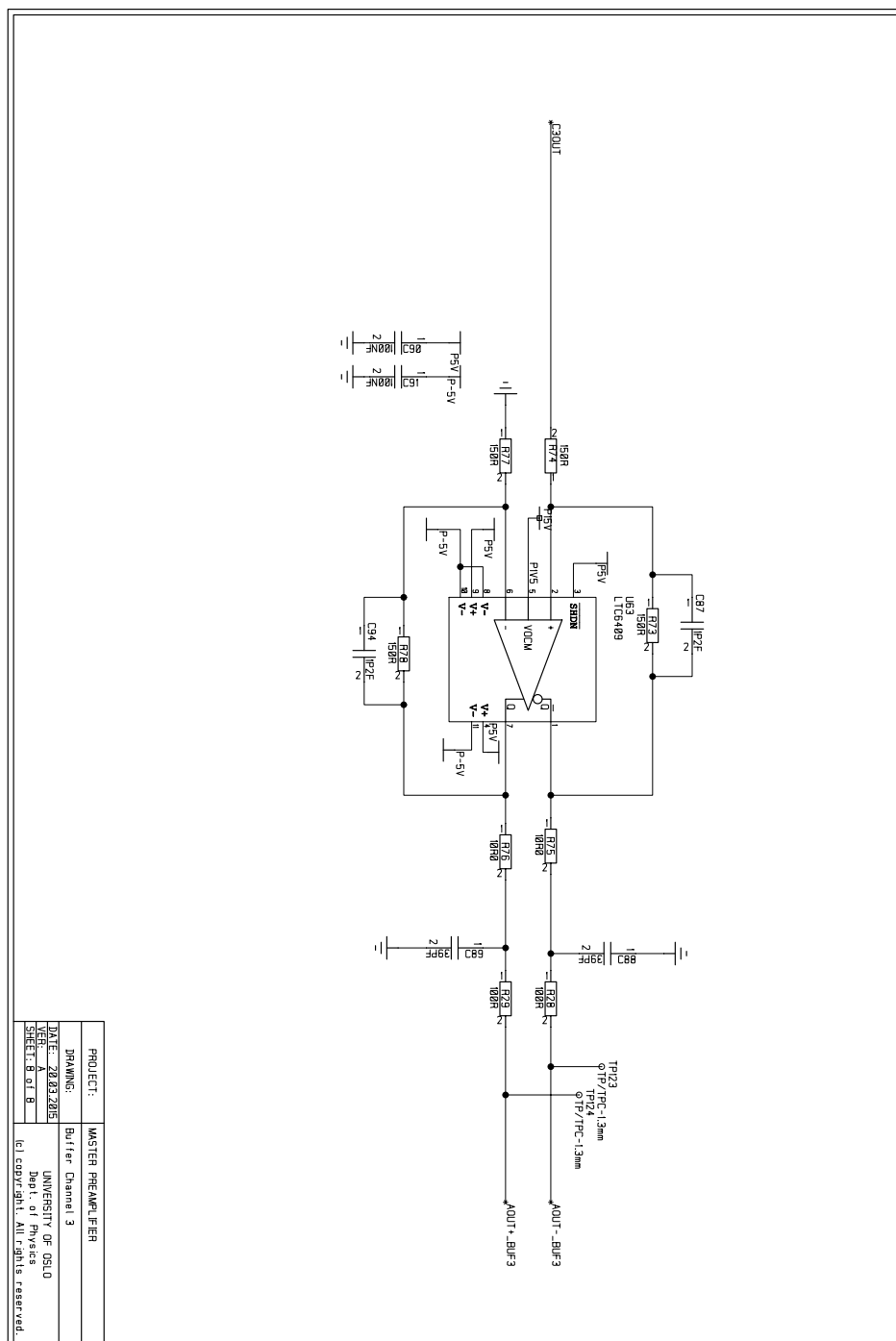




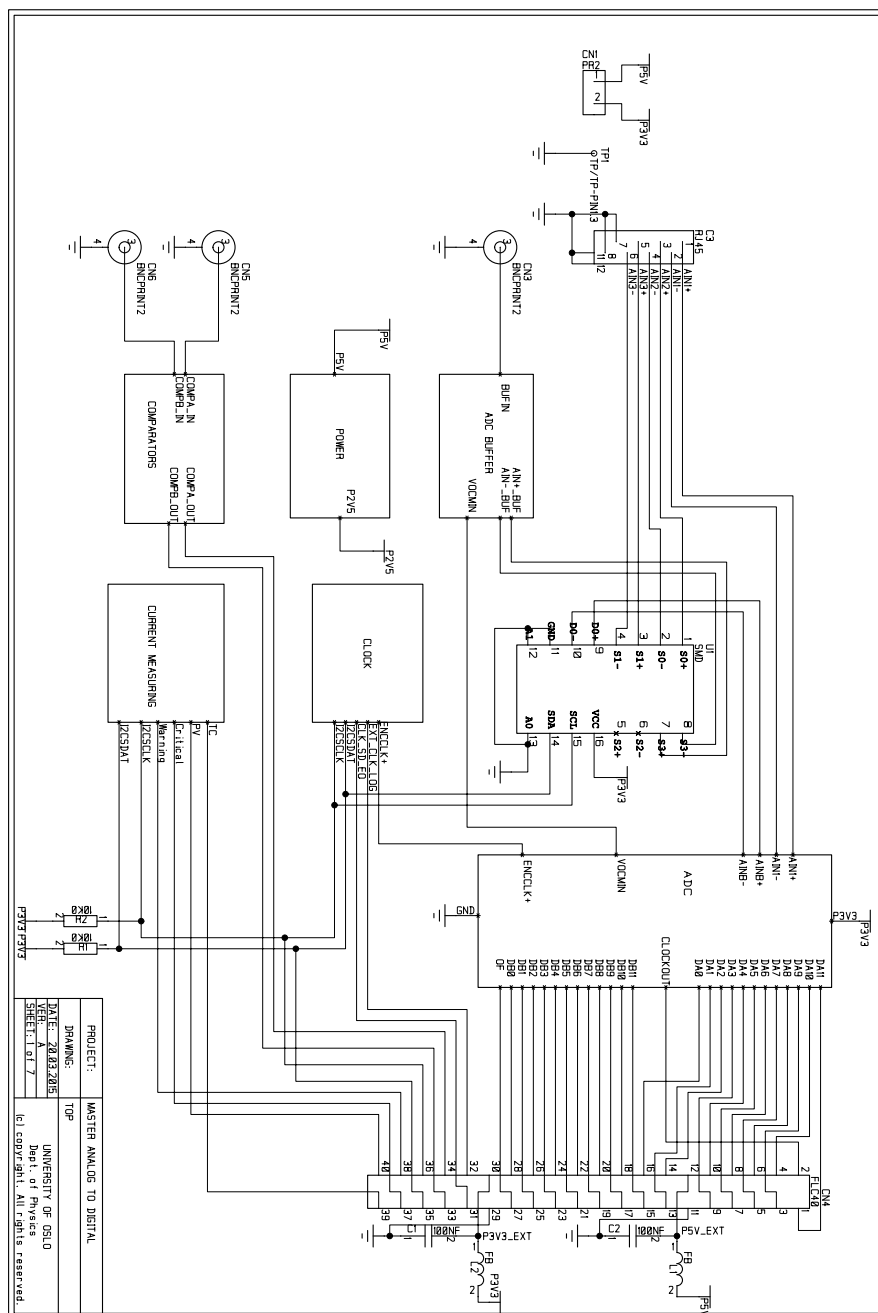


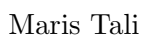


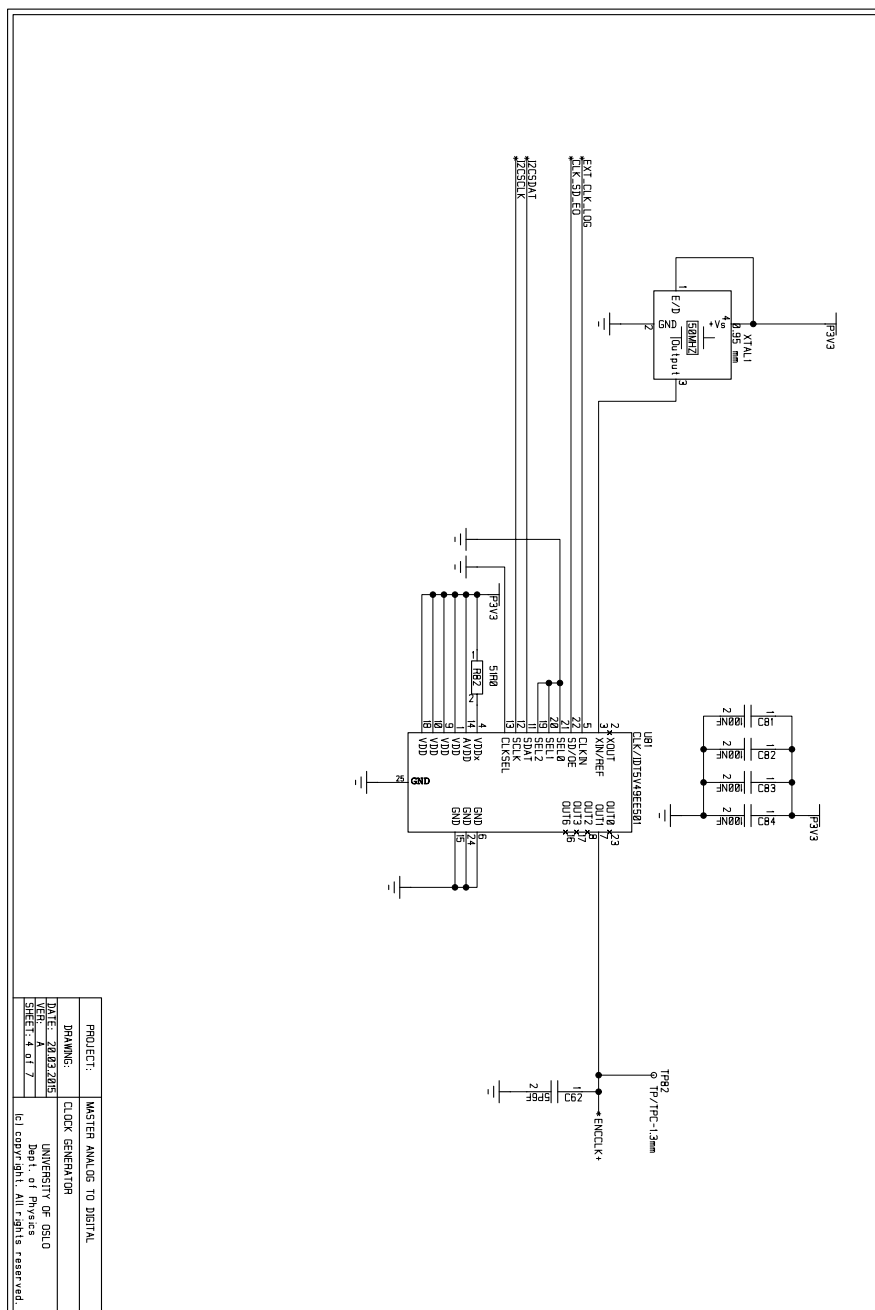


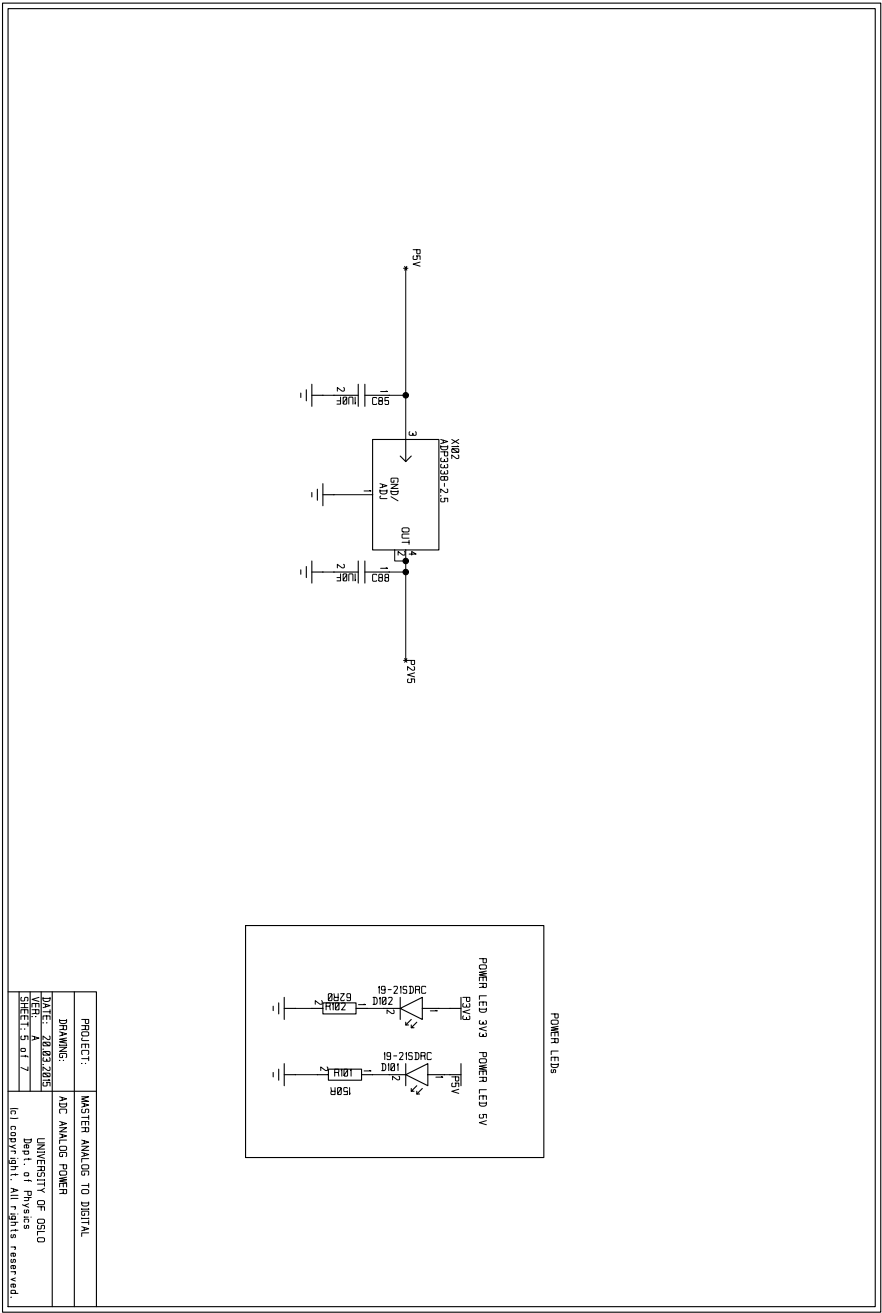


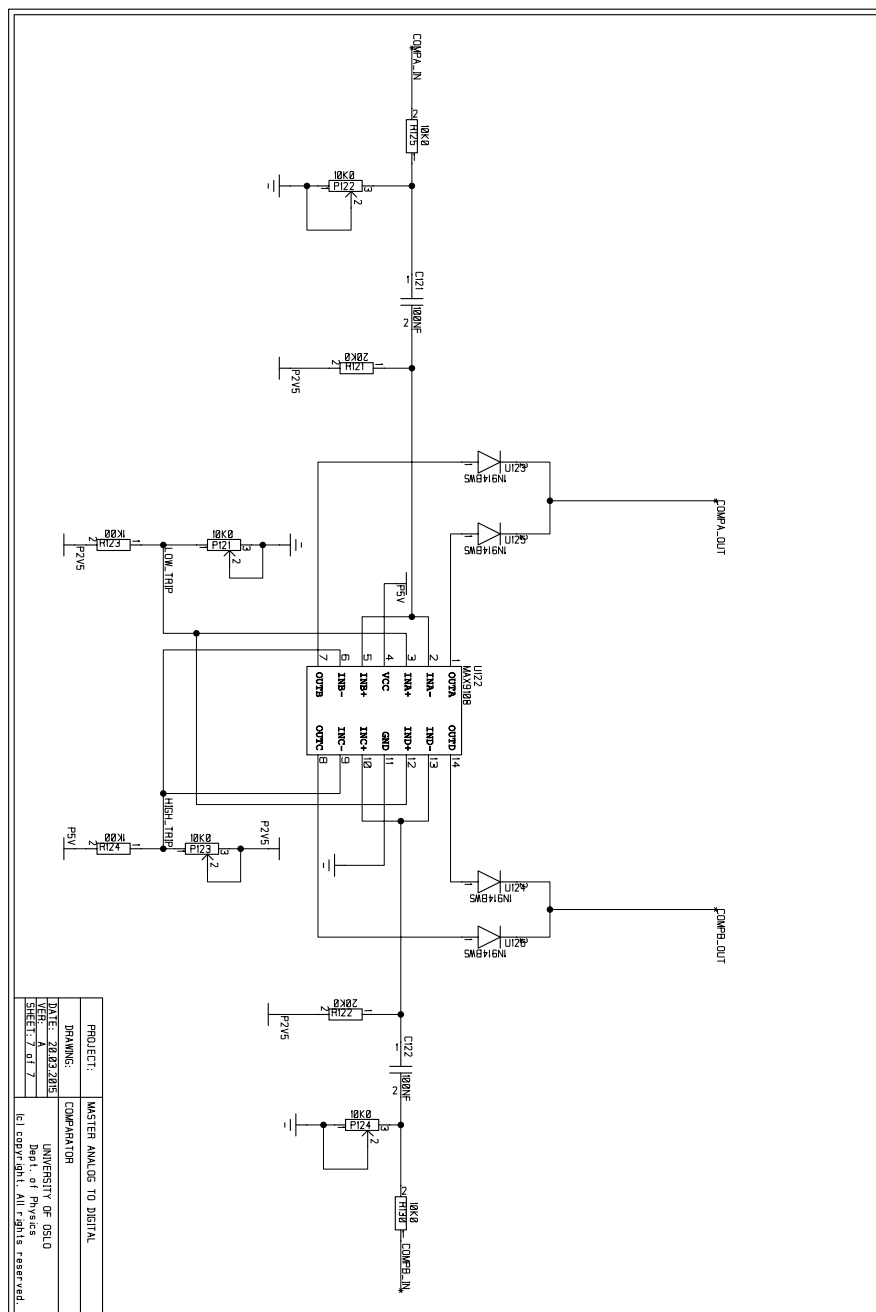
The complete schematics of the final analog PCB design











Appendix B

mux.c

```
#include <errno.h>
#include <string.h>
#include <stdio.h>
#include <stdlib.h>
#include <unistd.h>
#include <linux/i2c-dev.h>
#include <sys/ioctl.h>
#include <sys/types.h>
#include <sys/stat.h>
#include <fcntl.h>
#include <math.h>

int i2c_select_out(int file, char out){
    char buffer[1];
    int res;
    int nr = out;

    if(nr < 0 || nr > 3){
        printf("Selected_multiplexer_output_must_be_between_0..3.");
        printf("Selected_output:%d\n", nr);
        return 1;
    }
    buffer[0] = 0x08 + nr*2;
    res = write(file, buffer, 1);
    if(res < 1) {
        printf("Read_result_error:%s\n", strerror(res));
        return res;
    }
    printf("Selected_output%d\n", nr);
    return res;
}

int i2c_init_mux(){
    int file;
    char *filename = I2C_CHANNEL;
    if((file = open(filename, ORDWR)) < 0){
        perror("Failed_to_open_i2c_bus\n");
    }
}
```

```

        return 1;
    }

    //scan_i2c_bus(file);

    int addr = 0x4C;

    if(ioctl(file , I2C_SLAVE, addr) < 0){
        printf("Failed to talk to slave\n");
        return 5;
    }
    return file;
}

```


clock.c

```
//defines

/*    Clock levels    */
#define LVDS 0x01
#define LVTTL 0x00
#define LVPECL 0x10
#define HCSL 0x11
/*    Sources    */
#define PLL2 0x0c
#define REF 0x04
/*    PM settings    */
#define PM1 0x01
#define PM0 0x00
#define BIG_FLOAT 99999999
/*    Constraints    */
#define MIN_Q 1
#define MAX_Q 126
#define MIN_N 10
#define MAX_N 4095
#define MIN_D 1
#define MAX_D 127

#define XTAL 0x04
#define ICLK 0x0c

int calculate_clock_speed(int file , clocks* clock){
    int i;
    float q = 1;
    float n = 1;
    float d = 1;
    //reference speed from XTAL
    float speed = 50;
    for(i = 0; i < 6; i++){
        speed = 50;
        q = 1;
        n = 1;
        d = 1;
        if(clock > source[i] == REF){
```

```

        //printf("CFG%d source REF\n", i);
    }else if(clock > source[i] == PLL2){
        //printf("CFG%d source PLL2\n", i);
        n = clock > n2[i];
        d = (int)clock > d2[i];
    }else{
        printf("Clock_CFG%d_speed_can_not_be_calculated\n", i);
    return 1;
    }
    if((int)clock > q2[i] == 127){
        if(clock > pm2[i] == PM0) speed = 0;
        //else output is divided by 1
    }else{
        if(clock > pm2[i] == PM0){
            q = 2;
        }else{
            q = ((int)clock > q2[i]+2)*2;
        }
    }
    speed = speed*(n/d);
    speed = speed/q;
    //printf("Clock_CFG%d: %.02f MHz\n", i, speed);
    //printf("Clock_CFG%d: n=%.02f d=%d odiv=%.02f q=%.02f pm=0x%x source=%s\n",
    clock > speed[i] = speed;
}
return 1;
}

float set_clock_speed(int file, clocks* clock, int clk, float target){
    int n = 2;
    int q = 1;
    int d = 1;
    char pm;
    char source;
    int ret = 1, done = 0, easycalc = 0;
    float closest = BIG_FLOAT, result, fin = 50.;
    int i, j, k;
    int found = 0;

    if(clk < 0 || clk > 6){
        printf("Selected_clock_number_must_be_between_0..5.");

```

```

    printf("Currently_selected_clock:_%d\n", clk);
    return 1;
}else if(target > 250 || target < 0){
    printf("Error._Illegal_value_%.03f_for_clock_speed._", target);
    printf("Legal_values_for_clock_between_0..250\n");
    return 1;
}

printf("Target_speed:_%f_MHz.\n", target);
//find out if output could just be REF divided by q
float odiv = 6, diff = BIG_FLOAT;
for(i = 0; i < 127; i++){
    result = fin/odiv;
    diff = fabs(result - target);
    if(diff < closest) closest = result;
    if(diff < 0.001){
        easycalc = 1;
        break;
    }
    odiv += 2;
}

if(target == fin){
    //disable pll2
    d = 0;
    //set q to 127 and pm to 1 = divide out by 1
    q = 127;
    pm = PM1;
    //turn off PLL2
    d = 0;
    source = REF;
}else if(target == fin/2){
    //disable pll2
    d = 0;
    //set q to != 127 and pm to 0 = divide out by 2
    q = 1;
    //turn off PLL2
    d = 0;
    pm = PM0;
    source = REF;
}else if(easycalc == 1){

```

```

q = (odiv 4) / 2;
pm = PM1;
source = REF;
//turn off PLL2
d = 0;
//printf("Easycalc success.\n");
} else {
    float tolerance = 0.001;
    while(found != 1){
        for(i = MIN_N; i <= MAX_N; i++){
            for(j = MIN_Q; j <= MAX_Q; j++){
                for(k = MIN_D; k <= MAX_D; k++){
                    odiv = (j+2)*2;
                    result = (fin*((float)i/(float)k))/(float)odiv;
                    diff = fabs(result - target);
                    if(diff < closest) closest = result;
                    if(diff < tolerance){
                        n = i;
                        q = j;
                        d = k;
                        //printf("Found it! N%d Q%d D%d res%f\n", i, j, k, diff);
                        //break out of all fpr loops
                        j = MAX_Q;
                        k = MAX_D;
                        i = MAX_N;
                        found = 1;
                        break;
                    }
                }
            }
        }
    }
    if(!found){
        printf("Could not find clock with tolerance %.02f%%\n", tolerance*100);
        tolerance = tolerance*10;
        printf("Increasing tolerance to %.02f%%\n", tolerance*100);
    }
    printf("Setting clock %d speed to %.04f MHz\n", clk, closest);
    source = PLL2;
    pm = PM1;
}

```

```

while(ret > 0 && done == 0){
    ret = set_clk_pm2(file , clock , clk , pm);
    if(ret < 0) printf("ERROR. _Could_not_set_CGF_%d_PM2.\n" , clk);
    ret = set_clk_d2(file , clock , clk , d);
    if(ret < 0) printf("ERROR. _Could_not_set_CGF_%d_D2.\n" , clk);
    ret = set_clk_n2(file , clock , clk , n);
    if(ret < 0) printf("ERROR. _Could_not_set_CGF_%d_N2.\n" , clk);
    ret = set_clk_q2(file , clock , clk , q);
    if(ret < 0) printf("ERROR. _Could_not_set_CGF_%d_Q2.\n" , clk);
    ret = set_clk_source(file , clock , clk , source);
    if(ret < 0) printf("ERROR. _Could_not_set_CGF_%d_source.\n" , clk);
    ret = calculate_clock_speed(file , clock);
    if(ret < 0) printf("ERROR. _Could_not_calculate_CGF_%d_speed.\n" , clk);
    done = 1;
}
return ret;
}

```